University of Alberta

ANALYSIS AND DESIGN OF A SWITCHED CAPACITOR BASED POWER QUALITY CONDITIONER

By

Tarek Abdel Moneim Kandil

A thesis

submitted to the faculty of graduate studies and research

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering

Edmonton, Alberta

Fall 2004

Library and Archives Canada

Published Heritage Branch

395 Wellington Street
Ottawa ON K1A 0N4
Canada

Bibliothèque et Archives Canada

Direction du Patrimoine de l'édition

395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence
ISBN: 0-612-95950-3
Our file Notre référence
ISBN: 0-612-95950-3

The author has granted a non-exclusive license allowing the Library and Archives Canada to reproduce, loan, distribute or sell copies of this thesis in microform, paper or electronic formats.

The author retains ownership of the copyright in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque et Archives Canada de reproduire, prêter, distribuer ou vendre des copies de cette thèse sous la forme de microfiche/film, de reproduction sur papier ou sur format électronique.

L'auteur conserve la propriété du droit d'auteur qui protège cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou aturement reproduits sans son autorisation.

In compliance with the Canadian Privacy Act some supporting forms may have been removed from this thesis.

While these forms may be included in the document page count, their removal does not represent any loss of content from the thesis.

Conformément à la loi canadienne sur la protection de la vie privée, quelques formulaires secondaires ont été enlevés de cette thèse.

Bien que ces formulaires aient inclus dans la pagination, il n'y aura aucun contenu manquant.

Canada

DEDICATED TO MY PARENTS,

WIFE

AND CHILDREN

.....

Acknowledgement

First and foremost, I would like to thank and praise God almighty for enlightening my way and directing me through each and every success I have or may reach.

I would like to thank and express my appreciation to my supervisor, Dr. Wilsun Xu, for his encouragement and patience during my research work. It has been my honor and privilege to work under his supervision. His enthusiasm, guidance and insight throughout the duration of this study were invaluable to me.

I would like to extend my appreciation and deep thanks to Dr. Luiz Lopes, Concordia University, Montreal. I'm deeply indebted for my current achievements to the invaluable guidance I have been receiving from him. His advice, and critical discussions are the main factors that helped me to accomplish this work.

My gratitude and thanks goes to Dr. John Salmon for the useful discussions and help during this research work.

It has been a great opportunity to work with my colleagues in the power quality research group. I would like to thank all of them, especially Sami Abdulsalam, for their cooperation and fruitful discussions.

My thanks also goes to Albert Terheide for his endless support and solving most of the problems that I encountered during my work in the power system laboratory.

I would like to express my sincere gratitude, thanks, and love to my mother for her continuous encouragement and love during the period of study. I would like to extend my gratitude to my family to have their support and care all these years. I got mainly from them the strength and inspiration that enabled me to finish this work.

Finally, I would like to express my gratitude to my wife for her patience, care, and support through the most difficult periods of this work. To her goes a great part of my gratitude.

Contents

1. INTRODUCTION 1

1.1 INTRODUCTION 1

1.2 OBJECTIVES 4

1.3 CONTRIBUTIONS 4

1.4 ORGANIZATION OF THE THESIS 5

2. BACKGROUND 7

2.1 INTRODUCTION 7

2.2 TUNED OR TRAP FILTERS 8

2.3 ACTIVE FILTERS 8

2.3.1 Classification according to power rating and speed of response required in the compensated system 9

2.3.2 Classification according to compensated variables 11

2.3.3 Classification according to power circuit configuration and connections 13

2.3.4 Classification according control techniques 19

2.3.5 Classification according current/voltage reference estimation techniques 21

2.4 CONCLUSIONS 23

3. THE PROPOSED SCHEME AND STANDARD CONTROL STRATEGY 24

3.1 INTRODUCTION 24

3.2 PRINCIPLE OF OPERATION OF A SWITCHED CAPACITOR TOPOLOGY 25

3.2.1 Basic principle of Continuous Reactive Power Compensation 25

3.2.2 Principle of Continuous Reactive Power Compensation with Switched Capacitor (SC) 26

3.3 THE PROPOSED SCHEME 32

3.3.1 Power Structure and Standard Control Strategy 32

3.3.2 Designing the Proposed Topology 36

3.4 REACTIVE POWER COMPENSATION WITH THE PROPOSED SC SCHEME 43

3.4.1 Generation of the Reference Current for the Proposed Control Strategy 43

3.4.2 Design Procedure 48

3.5 SIMULATION RESULTS 53

3.6 LIMITATIONS OF THE PROPOSED SCHEME 57

3.7 EXPERIMENTAL SET UP 62

3.7.1 Power Circuit 62

3.7.2 Voltage and Current Sensing 63

3.7.3 Control Circuit 64

3.7.4 Dead-Time and Driving Circuits 66

3.7.5 Experimental Results 66

3.8 CONCLUSIONS 73

4. THE PROPOSED SCHEME AND MODIFIED CONTROL STRATEGY 74

4.1 INTRODUCTION 74

4.2 MODIFIED CONTROL STRATEGY 75

4.2.1 Modified Logic Circuit 75

4.2.2 Capacitor Voltages Regulation 78

4.3 DESIGNING THE SC SCHEME WITH THE MODIFIED CONTROL STRATEGY 82

4.3.1 Deriving Design Equations for the Modified Control Strategy *82*
4.3.2 Parameters Estimation *83*
4.4 SIMULATION RESULTS 85
4.4.1 Steady State Operation *85*
4.4.2 Transient Analysis *94*
4.5 EXPERIMENTAL SET UP 103
4.5.1 Control Circuit *103*
4.5.2 Experimental Results *106*
4.6 COMPARISON BETWEEN THE PROPOSED SC POWER CONDITIONER AND INVERTER-BASED POWER CONDITIONERS 116
4.7 CONCLUSIONS 119

5. APPLICATION EXAMPLE: SC BASED HARMONIC ACTIVE FILTER 120

5.1 INTRODUCTION 120
5.2 GENERATION OF THE REFERENCE CURRENT FOR THE PROPOSED CONTROL STRATEGY 121
5.2.1 Reference Current Generation Using Universal Active Filter (UAF) *121*
5.2.2 Reference Current Generation Using Adaptive Noise Canceling (ANC) Technique *124*
5.3 DESIGN PROCEDURE 125
5.3.1 General Considerations *125*
5.3.2 Calculating Circuit Components *126*
5.4 SIMULATION RESULTS 129
5.4.1 Simulation Results with Reference Current Generation Using UAF Technique *129*
5.4.2 Simulation Results with Reference Current Generation Using ANC Technique *135*
5.4.3 Comparison Between the Performance of the SC Scheme under the Two Reference Generation Circuits *140*

5.4.4 Transient Analysis *141*

5.5 EXPERIMENTAL SET UP 147

5.5.1 Power and Control Circuits *147*

5.5.2 Experimental results *149*

5.6 CONCLUSIONS 156

6. CONCLUSIONS AND FUTURE WORK 157

6.1 CONCLUSIONS 158

6.2 SUGGESTIONS FOR FUTURE WORK 161

6.2.1 Application of the SC Scheme for Three Phase System *161*

6.2.2 Application of the SC Scheme for Series Compensation *165*

6.2.3 Other Suggested Future Research Topics *165*

BIBLIOGRAPHY 166

A. CALCULATION OF THE CONSTANTS A_{1K} & A_{2K} FOR THE MATHEMATICAL CODE 175

B. MATLAB CODES FOR THE DESIGN PROCEDURE 178

List of Tables

Table 4.1 Comparison between the proposed SC power conditioner and inverter based power conditioners from the installation cost point of view for low power application. 117

Table 4.2 Comparison between the proposed SC power conditioner and inverter based power conditioners from the installation cost point of view for medium power application. 118

Table 5.1 Load current THD, source current THD, and switching frequency (F_s), for different types of simulation when using both UAF reference generation technique. 134

Table 5.2 Load current THD, source current THD, and switching frequency (F_s), for different types of simulation when using both ANC reference generation technique. 139

Table 5.3 Comparison between the performance of the SC scheme under UAF and ANC reference generation schemes. 140

List of Figures

Figure 2.1 Generalized block diagram for active power filters 9
Figure 2.2 Classification of active filters according to power circuit configuration and connection 14
Figure 2.3 Schematic representation of shunt active filter 14
Figure 2.4 Inverter based shunt active filter topology 15
Figure 2.5 Schematic diagram of one the of SC circuits. 16
Figure 2.6 Inverter based series active filter topology 17
Figure 2.7 System configuration of "series active-shunt passive" filter topology 18
Figure 2.8 System configuration of "shunt active-shunt passive" filter topology 18
Figure 2.9 System configuration of "series and shunt active filters" filter topology 19
Figure 2.10 Classification of active filters according to control techniques. 20
Figure 2.11 Classification of active filters according to current/voltage estimation techniques. 22
Figure 3.1 The principle of continuous control of KVar. 25
Figure 3.2 Switched capacitor filter with non-linear load. 26
Figure 3.3 Standard hysteresis control. 28
Figure 3.4 Different modes of operations for SC circuit. 29
Figure 3.5 Voltage at the point of common coupling and capacitor voltage waveforms. 30

Figure 3.6 Switched capacitor configurations. 31
Figure 3.7 Proposed switched capacitor based power conditioner. 34
Figure 3.8 Control circuit of the standard switching strategy 35
Figure 3.9 Circuit separation 37
Figure 3.10 Optimization procedure for selection of different filter parameters. 41
Figure 3.11 Adaptive noise canceling concept. 44
Figure 3.12 Scheme for generating the reference current of the power conditioner 46
Figure 3.13 Typical waveforms for the supply voltage v_{PCC}, capacitor voltages, v_{c1} & v_{c2} and the power conditioner's current i_f for 49
Figure 3.14 Optimization procedure results. 52
Figure 3.15 Main elements of the power circuit of SC power conditioner simulation system. 54
Figure 3.16 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c , and Voltage at the point of common coupling v_{pcc}, for a *linear inductive load.* 55
Figure 3.17 SC performance with an *inductive load* 56
Figure 3.18 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c , and Voltage at the point of common coupling v_{pcc}, for a *linear capacitive load.* 58
Figure 3.19 SC performance with a *capacitive load* 59
Figure 3.20 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c , and Voltage at the point of common coupling v_{pcc}, for *a diode bridge rectifier with capacitor filter load.* 60
Figure 3.21 SC performance with *a non-linear load* 61
Figure 3.22 Bi-directional switch. 63
Figure 3.23 Supply voltage sensing circuit 63
Figure 3.24 Load and filter currents sensing circuits. 64
Figure 3.25 Control circuit hardware for reactive power compensation. 65
Figure 3.26 (a) Experimental circuit that provide dead time between switches. (b) PSPICE simulation results for the dead-time circuit. 67

Figure 3.27 Driving circuit for an IGBT 68
Figure 3.28 Load current, power conditioner current, supply current and supply voltage respectively with (a) inductive load (L = 24 mH, R = 10 Ω), (b) capacitive load (C = 340 uF, R = 10 Ω)..... 69
Figure 3.29 Experimental waveforms for the supply voltage v_{s_n}, supply current i_s, and switching signals. 70
Figure 3.30 Experimental waveforms for the supply voltage v_s, capacitor voltages, v_{c1} & v_{c2}, and power conditioner current i_f for a capacitive reference current.. 70
Figure 3.31 (a) Load current, power conditioner current, supply current and supply voltage with rectifier bridge with capacitive filter load with standard control strategy,..... 72
Figure 4.1 Modified switching strategy for the power conditioner. 75
Figure 4.2 Modes of operation for the modified control strategy. 77
Figure 4.3 Modified Logic circuit implementation. 78
Figure 4.4 Capacitor voltage regulation by the modified control strategy. 79
Figure 4.5 The complete circuit implementation of the modified control strategy. 81
Figure 4.6 (a) Window of i_f, v_{pcc}, *and* v_{S1} across the zero crossing of v_{pcc} with *stanadard* control strategy, (b) Window of i_f, v_{pcc}, *and* v_{S1} across the zero crossing of v_{pcc} with *modified* control strategy. 86
Figure 4.7 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c, and v_{pcc}, for a linear inductive load..... 87
Figure 4.8 SC performance with an inductive load..... 88
Figure 4.9 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c, and v_{pcc}, for a linear capacitive load..... 89
Figure 4.10 SC performance with a capacitive load 90
Figure 4.11 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c, and v_{pcc}, for a diode bridge rectifier with capacitor filter load..... 91
Figure 4.12 Comparison between the harmonic spectrum for both the standard and modified control strategies with diode bridge rectifier and capacitor filter. 92

Figure 4.13 SC performance with an inductive load,..... 93
Figure 4.14 Response of the SC scheme with a step change in the reference current for: (a) Reference capacitive current (b) Reference inductive current. 95
Figure 4.15 Response of the SC scheme with a step change in the voltage for:..... 96
Figure 4.16 Response of the SC scheme with a step change in both the supply voltage and reference current for: (a) Reference capacitive current (b) Reference inductive current. 99
Figure 4.17 Response of the SC scheme with a step change in the power factor of 1.5 kVA load from 0.866 lagging to 0.866 leading. 100
Figure 4.18 Response of the SC scheme with a step change in the firing angle thyristor bridge rectifier with an inductive load, L_{dc} = 50.0 mH, R_{Load} = 5.0 Ω from 15° to 30°..... 102
Figure 4.19 Control circuit hardware for reactive power compensation. 104
Figure 4.20 Experimental set up of the logic circuit of the modified control strategy. 105
Figure 4.21 Load current, power conditioner current, supply current and voltage at the point of common coupling respectively with (a) inductive load (L = 24 mH, R = 10 Ω), (b) capacitive load (C = 340 uF, R = 10 Ω). 107
Figure 4.22 Experimental waveforms for the voltage at the point of common coupling $v_{pcc,}$ supply current i_s, and switching signals. 108
Figure 4.23 Experimental waveforms for the $v_{pcc,}$ capacitor voltages, v_{c1} & v_{c2} , and power conditioner current i_f for a capacitive reference current..... 108
Figure 4.24 (a) Load current, power conditioner current, supply current and v_{pcc} with rectifier bridge with capacitive filter load with modified control strategy, (b) Harmonic spectrum for both load and supply current. 110
Figure 4.25 (a) Load current, power conditioner current, supply current and supply voltage with rectifier bridge with inductive load with the modified control strategy, (b) Harmonic spectrum for both load and supply current. 111
Figure 4.26 SC scheme performance for a cyclic inductive load current variation. 112
Figure 4.27 SC scheme performance for a cyclic capacitive load current variation..... 113
Figure 4.28 SC scheme performance for a cyclic supply voltage variation. 114
Figure 4.29 SC scheme performance for a sudden change in the load power factor.... 115

Figure 5.1 (a) Circuit for reference current generation. (b) General form of the notch filter response. (c) Output waveform from the universal active filter chip when it has a square wave input waveform 122
Figure 5.2 Complete control circuit for the SC system used in harmonic mitigation... 123
Figure 5.3 Scheme for generating the reference current of the power conditioner..... 125
Figure 5.4 Typical waveforms for: (a) v_{pcc} and capacitor voltages, v_{c1} & v_{c2} (b) Load current i_L, filter current i_f, and source current i_s 127
Figure 5.5 Optimization procedure results. 128
Figure 5.6 (a) Simulation waveforms with UAF technique for a single-phase diode bridge rectifier circuit with capacitor filter: load current i_L , filter current i_f , source current i_s , and v_{pcc}, v_{c1} & v_{c2}. (b) Harmonic spectrum for the load and source currents..... 130
Figure 5.7 (a) Simulation waveforms with UAF technique for a single-phase diode bridge rectifier circuit with inductive load: load current i_L , filter current i_f , source current i_s , and v_{pcc}, v_{c1} & v_{c2}. (b) Harmonic spectrum for the load and source currents..... 132
Figure 5.8 (a) Simulation waveforms with UAF technique for a single-phase thyristor bridge rectifier circuit with inductive load: load current i_L , filter current i_f , source current i_s , and v_{pcc}, v_{c1} & v_{c2}. (b) Harmonic spectrum for the load and source currents..... 133
Figure 5.9 (a) Simulation waveforms with ANC technique for a single-phase diode bridge rectifier circuit with capacitor filter: load current i_L , filter current i_f , source current i_s , and v_{pcc}, v_{c1} & v_{c2}. (b) Harmonic spectrum for the load and source currents..... 136
Figure 5.10 (a) Simulation waveforms with ANC technique for a single-phase diode bridge rectifier circuit with inductive load: load current i_L , filter current i_f , source current i_s , and v_{pcc}, v_{c1} & v_{c2}. (b) Harmonic spectrum for the load and source currents..... 137
Figure 5.11 (a) Simulation waveforms with ANC for a single-phase thyristor bridge rectifier circuit with inductive load: load current i_L , filter current i_f , source

current i_s , and v_{pcc}, v_{c1} & v_{c2}. (b) Harmonic spectrum for the load and source currents. 138
Figure 5.12 Simulation results for transient response of the SC filter for a step increase and decrease in the *load current* at the tenth cycle and twentieth cycle respectively. 142
Figure 5.13 Simulation results for transient response of the SC filter for a step increase and decrease in the v_{pcc} at the tenth cycle and twentieth cycle respectively. 144
Figure 5.14 Simulation results for transient response of the SC filter for a step increase and decrease in the v_{pcc} at the tenth cycle and twentieth cycle respectively with a constant load current. 146
Figure 5.15 Control circuit hardware. 148
Figure 5.16 Load current, SC filter current, supply current and voltage at the point of common coupling with rectifier bridge with capacitive filter load, (b) Harmonic spectrum for both load and supply currents. 150
Figure 5.17 Experimental waveforms for the voltage v_{pcc}, capacitor voltages, v_{c1} & v_{c2}, and SC filter current i_f. 151
Figure 5.18 (a) Load current, SC filter current, supply current and voltage at the point of common coupling with rectifier bridge with inductive load, (b) Harmonic spectrum for both load and supply current. 152
Figure 5.19 SC scheme performance for a cyclic load current variation. 154
Figure 5.20 SC scheme performance for a cyclic supply voltage variation. 155
Figure 6.1 System configuration of the proposed active filter scheme. 161
Figure 6.2 Operation of the switched capacitor filter with the proposed control strategy for a diode bridge rectifier with capacitive filter load. 163
Figure 6.3 Operation of the switched capacitor filter with the proposed control strategy for a diode bridge rectifier with inductive load. 164
Figure 6.4 Principle of series active filter technique. 165

CHAPTER 1

Introduction

1.1 Introduction

Today, the situation on AC systems has become a serious concern. In addition to external disturbances, such as outages, sags and spikes due to switching and atmospheric phenomenon, there are inherent, internal problems specific to each site, resulting from the combined use of linear and non-linear loads. Untimely tripping of protection devices, harmonic overloads, high levels of voltage and current distortion, temperature rise in conductors, transformers and generators all contribute to reducing the quality and the reliability of AC systems. The above disturbances are well understood and directly related to the proliferation of loads consuming non-sinusoidal current, referred to as "non-linear loads". This type of load is used for the conversion, variation and regulation of electrical power in commercial, industrial and residential installations. Moreover, recent studies show that the consumption of non-linear loads will sharply increase in the years to come [1].

With the increasing numbers of non-linear loads appearing in electricity supply networks, utility companies are now restricting negative effects by imposing strict limitations on the combined effects these loads impose on their systems. The benefits of

increased demands on the system are thus offset by problems with the local electric utility with regard to maintaining power quality limits. Generally speaking, disturbances phenomena in the power supply system become more pronounced with more number of non-linear loads. Consequently, power-conditioning equipment is becoming more important for electric utilities and their customers.

The control or mitigation of the power quality problems may be realized through the use of harmonic filters. Harmonic filters, in general are designed to reduce the effects of harmonic penetration in power systems and should be installed when it has been determined that the recommended harmonic content has been exceeded. Shunt passive filters have been widely used by electric utilities to minimize the harmonic distortion level [2,3]. They consist of passive energy storage elements (inductors and capacitors) arranged in such a way to provide a low impedance path to the ground just for the harmonic component(s) to be suppressed. However, harmonic passive filters cannot adjust to changing load conditions; they are unsuitable at distribution level as they can correct only specific load conditions or a particular state of power system [4,5].

Due to the power system dynamics and the random-like behavior of harmonics, consideration has been given to power electronic equipment known as an active power filter. An active power filter is simply a device that injects equal but opposite distortion into the power line, thereby canceling the original power system harmonics and improving power quality in the connected power system. This waveform has to be injected at a carefully selected point in a power system to correct the distorted voltage and current waveforms. The power converter used for this purpose has been known by different names such as: active power filter and active power line conditioner. The rating of the power converter is based on the magnitude of the distortion current and operated at switching frequency dedicated by the desired filter bandwidth. In addition to its filtering capability, this power converter can be used as a static var compensator (Statcom) to generate a dynamic capacitive or inductive current to compensate for the reactive power drawn from the load and to compensate for other disturbances such as voltage flicker.

Although, the concept of active power filtering was first introduced in 1971 by Sasaki and Machida who proposed implementation based on linear amplifiers [6], and

further improved in 1976 by Gyugyi et.al, who proposed a family of active power filter systems based on PWM current source inverters (CSI) and PWM voltage source inverters [7], these designs remained either at the concept level or at laboratory level due to the lack of suitable power semiconductor devices.

Due to recent developments in the semiconductor industry, power switches such as the insulated gate bipolar transistor (IGBTs) with high power rating and the capability of switching at high frequency, are available on the market. This makes the application of active power filters at the industrial level feasible. Several active power filter design topologies have been proposed. They can be classified as:

- Shunt active power filter [8].
- Hybrid Shunt active filter [9].
- Series active power filter [10].
- Hybrid series active power filter [11].

However, there are some major drawbacks associated with the inverter based active filters that may limit their operations. First, they usually employ relatively large dc-link capacitors, which increases the cost of the filter [12]. Moreover, the switching frequency of these filters is in the range of 20-30 kHz, which results in increased switching losses [13]. Finally, the three-phase inverter performance tends to deteriorate for unbalanced load currents or unsymmetrical supply voltages, especially in three-phase four-wire distribution systems. Three single-phase inverters may provide a better performance at the expense of cost increases [14].

As an alternative to overcome some of these problems, topologies based on switched capacitor (SC) filters and lattice structures have been proposed [15-18]. They offer good performance in terms of mitigation of harmonic distortion with smaller capacitor size and lower switching frequency. However, their control circuits are rather complicated requiring optimization techniques for the generation of gating signals. Further, they are not suitable for online control especially for systems that requires fast response due to high computation time.

1.2 Objectives

The main objective of this research is to develop and design a practical power conditioner solution capable of enhancing the power quality in distribution systems. The proposed device offers the potential of responding quickly to the changes in the system characteristics and is suitable therefore for on-line applications. This research is motivated by the lack of suitable existing power conditioning techniques and the demand for high filtering performance. The main topics can be outlined as follows:

- Development of circuit topology based on switched capacitor approach that is suitable for online control for distribution systems.
- Development of an effective mathematical model that can be used for the determination of different circuit parameters.
- Development of an easy reactive power compensation and harmonic mitigation strategy, which reduces the switching frequency requirements of the proposed power conditioner.
- Limiting the voltage across the capacitors to a range of relatively low values to reduce switches stresses.
- Development of control principles to implement the filtering strategy.
- Investigating the transient performance of the scheme under different conditions in the load and supply.
- Complete design of the active filter module

1.3 Contributions

Several aspects of this research work are novel and distinct from previous work done in related areas.

- A new single-phase power conditioner that is based on switched capacitor technology is presented. It presents a simple power structure and can be used for online application. This approach allows the use of low switching frequency and small rating switched capacitor circuit to achieve harmonic isolation and reactive power compensation.

- The proposed power conditioner operates with small passive elements that reduce the cost of the scheme.
- A systematic optimization procedure that is based on a detailed code for simulating currents and voltages in the circuit is used to determine the system components for different applications.
- A control circuit that is completely based on analog components is used to reduce the delay time introduced by digital circuits.
- A new control strategy for the standard hysteresis control is presented. It provides an alternative switching scheme for hysteresis control that allows an increase in the current tracking capability of the scheme at the worst possible case for switched capacitor topologies: the zero crossing points of the ac line voltage.
- With the low rating and low switching frequency characteristics, the proposed power conditioner system has the potential for applications at the distribution level of the utility grid.

1.4 Organization of the Thesis

The contents of the thesis is organized in the following manner:

Chapter 2 presents a literature review of the principle of operation of various power quality-conditioning schemes. Power circuit configurations of these systems along with their control strategies, advantages and disadvantages are presented in this chapter.

Chapter 3 describes the concept of the proposed switched capacitor based power conditioner along with its standard control strategy. Further, a mathematical model for the scheme that is used to determine the circuit parameters is presented. Finally, the limitations associated with the proposed scheme while performing its function, reactive power compensation and harmonic mitigation, are emphasized. Simulation and experimental results are provided to prove the effectiveness of proposed power circuit and the design methodology.

Chapter 4 presents a modified switching scheme that aims to mitigate some of limitations presented by the standard hysteresis control presented in Chapter 3. In addition, simulation results to evaluate the performance of the SC filter under steady state and transient operations to verify the effectiveness of the SC scheme and the design methodology are presented. Finally, experimental verification with a laboratory prototype for the modified scheme is presented.

Chapter 5 focuses on the application of the SC scheme in harmonic mitigation. Two reference current generation methods that are easy to implement and can provide the reference current with fast response, are chosen for generating the reference current for compensating harmonic currents for a given load. Steady-state operation and transient analysis are carried out to analyze the performance of the scheme under different operating condition. Finally, experimental results are provided to demonstrate the validity of the analysis and design procedure.

Chapter 6 summarizes the contribution of the research. Suggestions for future research work are also included.

CHAPTER 2

Background

2.1 Introduction

The flow of harmonics and reactive currents adversely affects the power system by lowering the power factor and deteriorating the voltage quality. These harmful effects are becoming increasingly more important for the following reasons:

- While the power demand is growing, public concerns over environmental impacts of transmission lines and right of way costs are making it more difficult for utility companies to build new transmission lines. The need to build new lines is reduced if the current carrying capacity of the existing transmission facilities is fully utilized by improving the power factor.
- Deregulation of the power industry is putting additional pressure on the utility companies to remain competitive by improving the voltage quality and by reducing the costly system losses.
- Addition of harmonics generating loads such as power electronics equipment by consumers is increasing the level of harmonic current flow in power system.

As a consequence to the economical significance of efficient power, a large number of researchers have discussed this subject and power-conditioning equipment becomes more important for electric utilities and their customers.

A literature review of the principle of operation of various power quality conditioning schemes along with their control strategies, advantages, and disadvantages is presented in this chapter.

2.2 Tuned or Trap Filters

Currently, the most widely used method for harmonic mitigation is the trap filter (passive shunt connected filter) that has dominated because of its low cost, reliability and simplicity, especially with one specific load power [1]. However, as their name implies, they require tuning to a specific harmonic frequency. Their effectiveness is marginal unless multiple tuned elements are incorporated. Moreover, this kind of compensator cannot solve random variations in the load waveform, and is susceptible to series and parallel resonance with the source impedance. As well, its compensation characteristics are highly sensitive to the changes of the neighboring loads and the utility impedance variations [2].

2.3 Active Filters

Figure 2.1 shows the components of a typical active power filter system and their interconnections. The information regarding the harmonic current generated by a non-linear load, for example, is supplied to the reference current/voltage estimator together with information about other system variables. The reference signal from the current estimator, as well as other signals, drives the overall system controller. This in turn provides the control for the PWM pattern generator. The output of the PWM pattern generator controls the power circuit via a suitable interface. The power circuit in the generalized block diagram can be connected in parallel, series, or parallel/series configurations, depending on the connection transformer used.

On the basis of the above, the published work in this field can be classified using the following criteria:

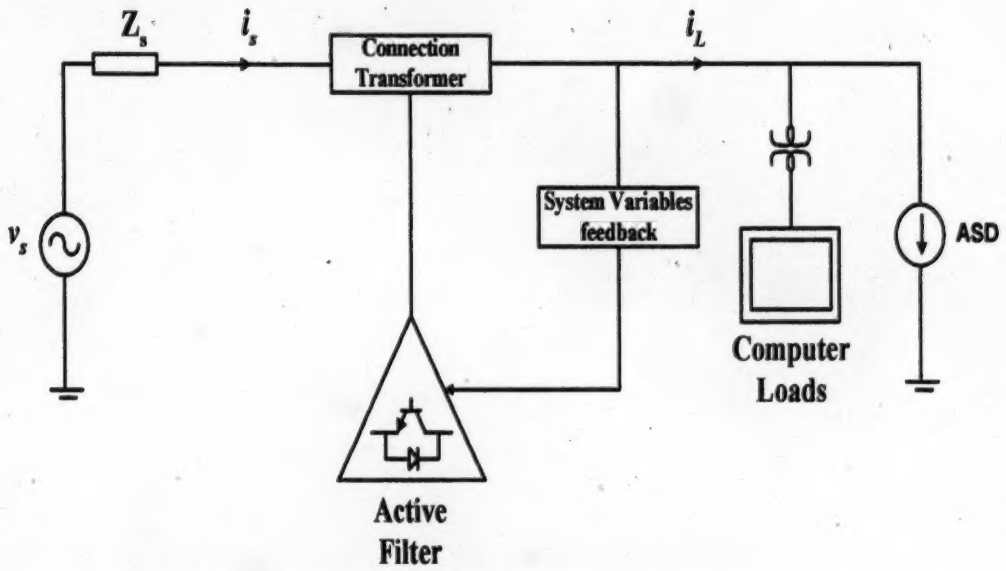


Figure 2.1 Generalized block diagram for active power filters

a- power rating and speed of response required in compensated systems,

b- power circuit configuration and connections,

c- system parameters to be compensated (e.g. current harmonics, power factor, etc,

d- control techniques employed, and

e- techniques used for estimating reference current/voltage.

The following sections classify the system according to the above criteria. This will provide a better understanding in dealing with these systems, as it shows the merits and drawbacks of each type.

2.3.1 Classification according to power rating and speed of response required in the compensated system

The power rating of the compensated system and its speed of response play a major role in deciding the control philosophy to implement the required filter. These two factors follow a reciprocal relationship [19-21]. In general, the cost of any particular system is proportional to the required speed of response [21].

2.3.1.1 Low power applications

This type of application is mainly concerned with systems of power ratings below 100 kVA. It is mainly associated with residential areas, commercial buildings, hospitals, and for a wide range of applications employs sophisticated techniques of dynamic active filters, especially those with high switching frequency voltage or current source inverters. Their response time is much faster than other techniques, rating from tens of microseconds to milliseconds and resulting in a considerable reduction in the power compensation range as stated above. This type comprises two categories:

- ***Single-phase systems***: They are generally available in low power ratings [22--33]. They are suitable for retrofit application, such as in commercial or residential buildings with computer loads [34], small factories, etc., where the current can be dealt with at the point of common coupling. The main advantage of these kinds of filters is that they can be operated at relatively higher frequencies, as they dealt with low power, leading to improved performance. However, in the absence of compulsory harmonic regulations [35-37], residential customers are not likely to invest in single-phase active filters.

- ***Three-phase systems:*** For three-phase applications the choice of filters depends on whether the three-phase are balanced or not. For balanced loads, a single three-phase inverter can be employed [38-55]. This is acceptable if there is no requirement to balance currents or voltages in each phase and aim is simply to eliminate as many harmonic currents as possible, assuming that the magnitudes and respective phase angels in each phase are the same. For unbalanced load currents or unsymmetrical supply voltages, especially three phase four wire systems; three single-phase inverters circuits [10] or alternative configurations [29-33] may provide acceptable solutions. These alternative configurations are discussed later in this chapter.

2.3.1.2 *Medium power applications*

In this category three phase systems ranging from 100 kVA to 10 MVA are mainly considered [56]. Medium to high voltage distribution systems and high power high voltage drive systems, where the effect of unbalance is negligible, fall within this classification. Here the main aim is to eliminate or reduce the current harmonics. Because of economic considerations, reactive power compensation using active filters at the high voltage distribution level is not generally regarded as viable [20], because of the high voltage and its accompanying problems of isolation and series/parallel connections of switches. Alternative approaches, including line commutated thyristor converters and tunable harmonic filters are considered more suitable [57-59].

2.3.1.3 *High power applications*

The implementation of very high power dynamic filters is extremely cost ineffective, because of the lack of the high frequency power devices that can control the current flow at such power rating, is a major limitation for such systems [60,61].

2.3.2 Classification according to compensated variables

Active filters are built to improve some of the characteristics of power systems under question. These characteristics are signified by the system parameters to be controlled, leading to the subdivisions discussed in the following sections.

2.3.2.1 *Reactive power compensation ('VAR' correction)*

Most researchers regard reactive power compensation as not requiring active filters [41-43,45,50]. However, compensation of power factor in conjunction with current harmonics is fairly popular and is addressed by many publications. On the other hand, active filter configurations rarely treat the problem of power factor correction on its own, owing to the fact that other quasi-dynamic cheaper and slower-in-response reactive-power compensators are available in the market. This technique (in this case called active-power filter for

reactive power compensation), if applied, would normally be suited for low power applications, since the currents needed for reactive power compensation are the same magnitude as the rated current of the load.

2.3.2.2 Harmonic compensation

This is the most important parameter requiring compensation in power systems and it is subdivided into current and voltage harmonic compensation as follows:

- ***Compensation of current harmonics:*** Compensation of current harmonics is a very important issue for low and medium power applications and is covered by many publications [19-21,29-33,59-60]. As mentioned above, the compensation of current harmonics reduces to great extent the amount of distortion in the voltage at the point of common coupling. The magnitude of the current and its waveform determines many of the power system design criteria. It is always recommended that the RMS value of the total current be reduced as much as possible (to reduce cable and feeder losses). The imposition of harmonic standards will soon oblige factories and establishments to control the amount of harmonics they inject into the power system [36,37].
- ***Compensation of voltage harmonics:*** The subject of compensating voltage harmonics is not widely addressed because power supplies usually have low impedance [28,44]. The terminal voltage at the consumer point of common coupling (PCC) is normally maintained within the standard limits for voltage sag and total harmonic distortion and doesn't normally vary much with loading. This problem is usually important for harmonic voltage sensitive devices, which require the supply to be purely sinusoidal, such as power system protection devices. It is worth mentioning that the compensation of voltage and current harmonics is interrelated. The reduction of voltage harmonics at the PCC helps a great deal to reduce current harmonics, especially for the particular cases of non-linear loads with resonance at the harmonic frequencies. However, the compensation of the voltage harmonics at the PCC does not eliminate the need for current harmonic compensation for non-linear loads.

- ***Harmonic currents with reactive power compensation:*** The most common and popular filters are those which compensate for both the reactive power and the harmonic currents in order to maintain the supply current completely free of harmonics and in phase with the supply voltage [22-24,52,53,62-66]. These techniques have several advantages over other alternatives, as only one filter is needed to compensate for everything, which is much more attractive than using different types of compensators. However, because of the limits imposed by the ratings of the power switches, one can only use this application for low power application. The resulting switching frequencies would need to be lower for higher-power applications, which restrict the filter under consideration to small powers.

2.3.3 Classification according to power circuit configuration and connections

Power circuit configurations play an important role in the selection of the applications, as some circuits are suitable only for certain aspects of control and power ranges, as discussed in this section and illustrated in the block diagram shown in figure 2.2.

2.3.3.1 Shunt active filters

This class of filter configurations constitutes those most important and most widely used in industrial processes [59-65]. It is connected to the main power circuit, as shown in the single line diagram of figure 2.3. The purpose is to cancel the load current harmonics fed to the supply. It can also contribute to reactive power compensation and balancing of three phase currents, as mentioned above. Shunt filters have the advantages of carrying only the compensation current. It is also possible to connect several filters in parallel to cater for higher currents, which makes this type of circuit suitable for a wide range of power ratings. This configuration consists of two main categories of

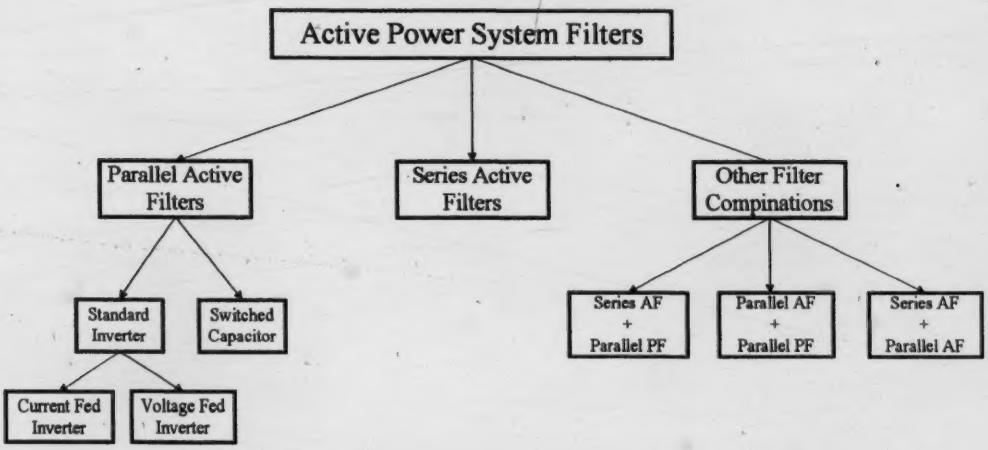


Figure 2.2 Classification of active filters according to power circuit configuration and connection

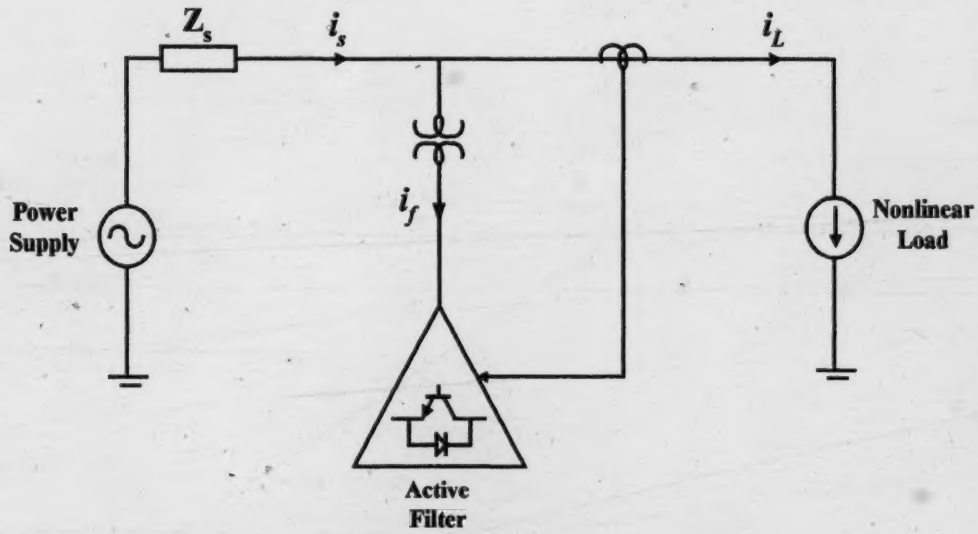


Figure 2.3 Schematic representation of shunt active filter

circuits, namely inverter-based configurations and switched-capacitor-based configurations. Information of these categories is discussed below.

- ***Inverter-Based shunt active filter:*** The basic block of an inverter based active filter is shown in figure 2.4. Most of the proposed topologies employ dc-ac converters (inverters) with IGBTs as semiconductor power switch and DSP for control purposes [21-25, 42, 49-53, 65]. On the one hand, this results in compactness, flexibility and better performance than passive filters but, on the other hand, it results in higher costs. However, there are some major drawbacks associated with the inverter based active filters that may limit their operations. First, they usually employ relatively large dc-link capacitors (4000-9000μF), which increase the cost of the filter [66]. In addition, they have the inherent disadvantage that the DC voltage bus has to be regulated for proper performance, which may complicate the control circuit. Moreover, the switching frequency of these filters is in the range of 20-30 kHz, which increases the switching losses [12]. Finally, the three-phase inverter performance tends to deteriorate for unbalanced load currents or unsymmetrical supply voltages, especially in three-phase four-wire distribution systems. Three single-phase inverters may provide a better performance at the expense of cost increase [67].

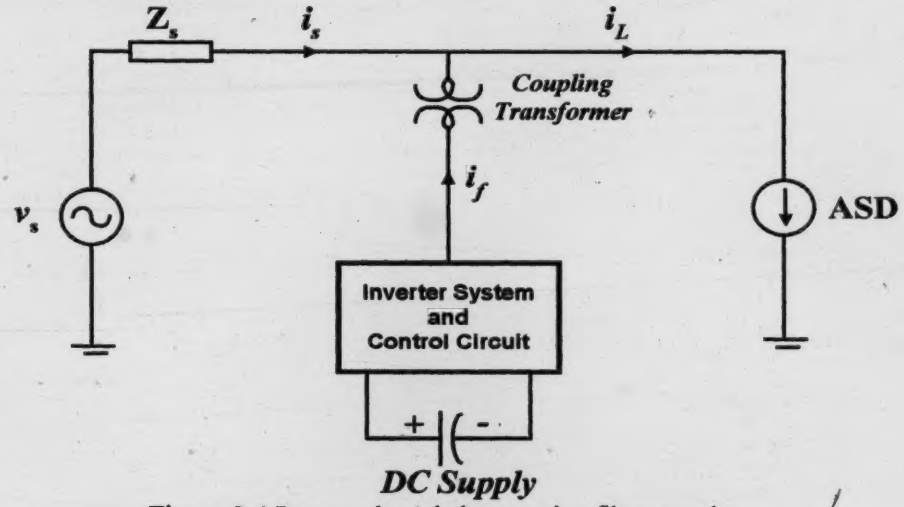


Figure 2.4 Inverter based shunt active filter topology

- ***Switched capacitor (SC) based shunt active filter:*** As an alternative to overcome some of inverter based active filters problems, topologies based on SC filters and lattice structures have been proposed [15-18, 68]. One of the proposed SC schemes is shown in figure 2.5. They offer good performance in terms of mitigation of harmonic distortion with smaller capacitor size and lower switching frequency. Therefore, they can be used of for high power applications. Further discussion on the principle of operation of this topology and different other configurations will be provided in the next chapter.

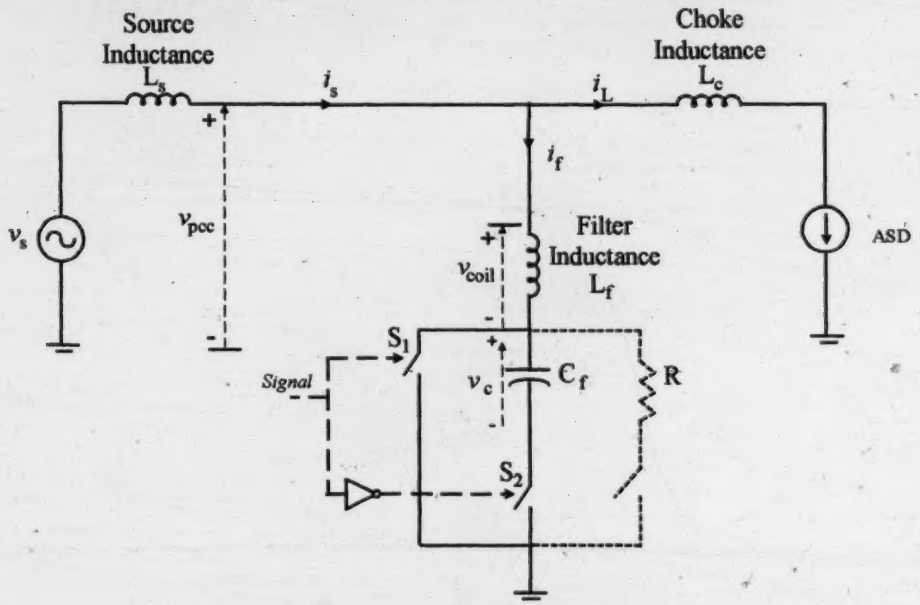


Figure 2.5 Schematic diagram of one the of SC circuits.

2.3.3.2 Series active filters

Figure 2.6 shows the basic block diagram of a stand-alone series active filter. The active filter in this configuration produces a PWM voltage waveform, which is continuously added/subtracted to/from the supply voltage to maintain a pure sinusoidal voltage waveform across the load [10,56-59]. The inverter configuration accompanying such a system is a voltage fed inverter without any current control loops. Series active filters are less common industrially than their rivals, shunt active filters. This is because of the main drawback that they

have to handle high currents, which increases their current rating compared with shunt filters, especially in the secondary side of the coupling transformer. The main advantage of series active filter is that they are ideal for eliminating voltage-waveform harmonics. It can provide the load with a pure sinusoidal waveform, which is important for voltage sensitive devices such as protection devices [26,28,43,45].

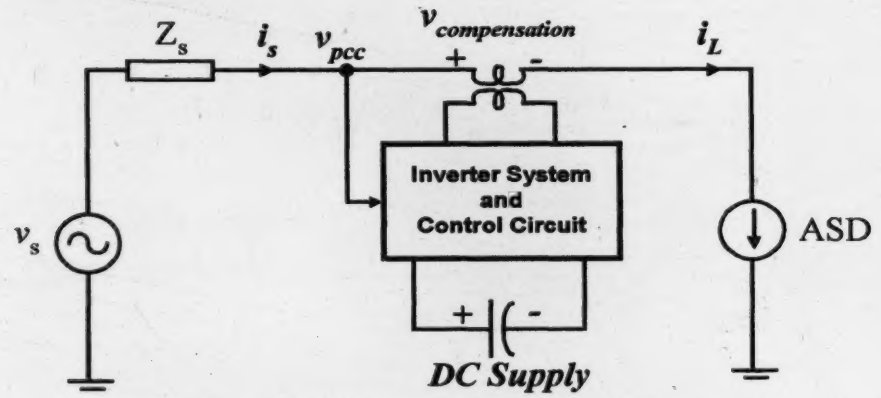


Figure 2.6 Inverter based series active filter topology

2.3.3.3 Other filter combinations

Combinations of several types of filter can achieve greater benefits for some applications

- ***Combination of series active and shunt passive filters:*** To reduce the complexity of the previous filter combination, a shunt passive filter to provide a path for harmonic currents of the load accompanies the inverter type series active filter, which theoretically constitutes infinite impedance for high frequency harmonics [69-71]. This kind of filter is quite popular because the solid-state devices used in the active series part can be of reduced size and cost (about 5% of the load size) and a major part of this combination is made of passive shunt L-C filter used to eliminate lower order harmonics [72]. This combination, represented by figure 2.7, permits an improvement over the characteristics of plain series active filters and the extension of their capabilities to include current harmonic reduction and voltage harmonic elimination.

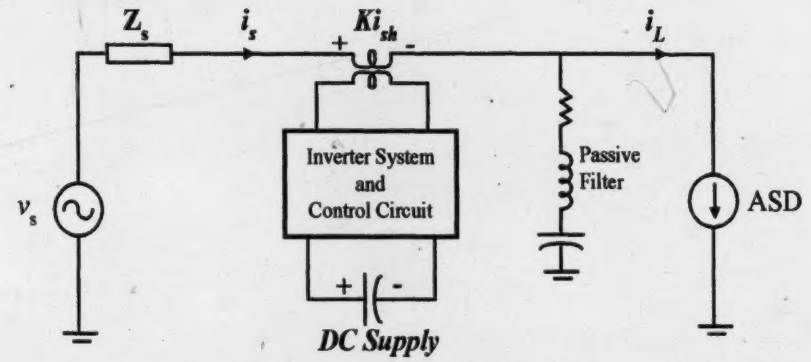


Figure 2.7 System configuration of "series active-shunt passive" filter topology

- ***Combination of shunt active and passive filters:*** This combination shown in figure 2.8 represents a very important mixture of passive and active inverter-type filters. The active filter is designed to eliminate only part of the low order current harmonics while the passive filter is designed to eliminate the bulk of the load-current harmonics. In such combinations, the system can be designed for higher powers without excessive costs for high-power switching [47,72]. The main drawback of this technique is that it contains too many power components, especially for the passive filter. Since the passive filter is always connected to the system, this approach is only suitable for a single load with a predefined harmonic source.

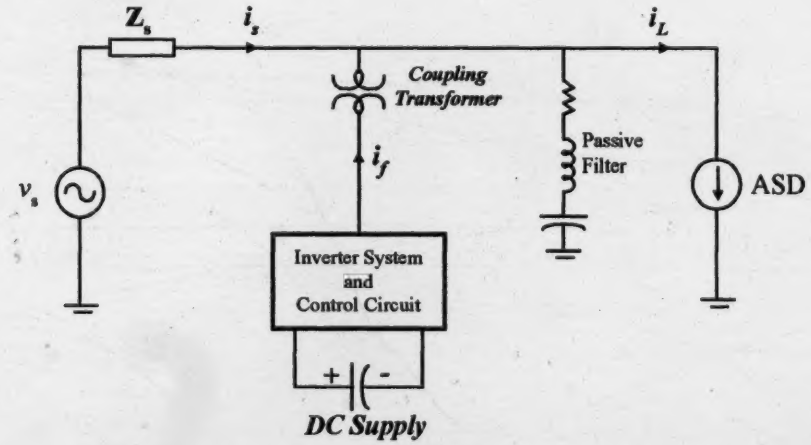


Figure 2.8 System configuration of "shunt active-shunt passive" filter topology

- ***Combination of series and shunt active filters:*** This configuration is known as "universal active filter" and its power circuit is shown in figure 2.9. The dc-link element is hared between two inverters operating as active series and active shunt compensators [73-75]. It is considered an ideal active filter, which eliminates voltage and current harmonics and is capable of giving clean power to critical and harmonic loads. However, its main drawbacks are its large cost and control complexity because of large number of solid-state device involved.

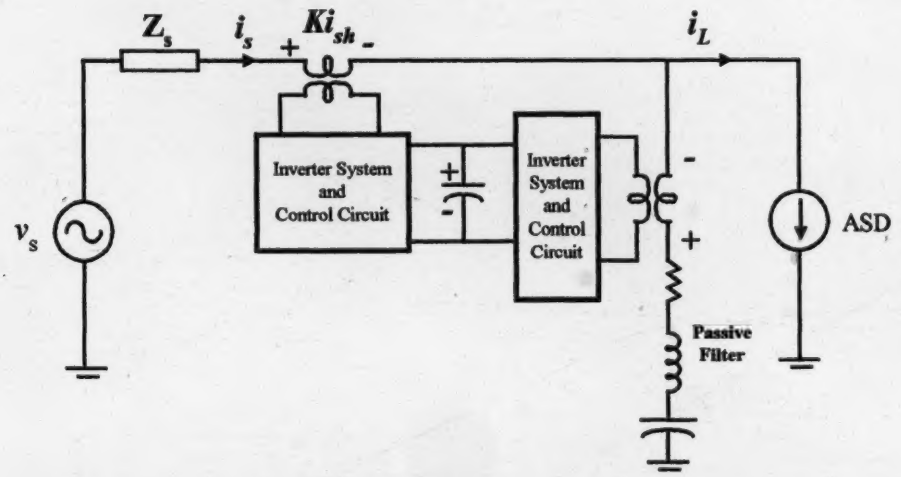


Figure 2.9 System configuration of "series and shunt active filters" filter topology

2.3.4 Classification according control techniques

Figure 2.10 shows a convenient method of classifying the presently available control techniques. These techniques fall into the main categories of open loop and closed loop controls. The closed loop controls can be further subdivided into other techniques as shown in figure 2.10.

2.3.4.1 Open loop control systems

Open loop systems sense the load current and the harmonics it contains. They simply inject a fixed amount of power in the form of current (mainly reactive) into

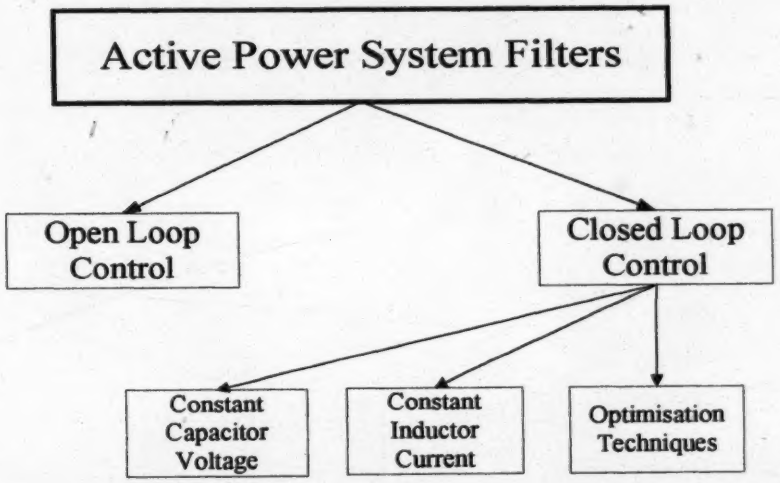


Figure 2.10 Classification of active filters according to control techniques.

the system, which may compensate for most of the harmonics and/or reactive power available. These systems do not check how successful the compensation has been. This has been the case with some of the traditional filtering techniques. Such techniques may include switched passive filter banks, systems with known constant load harmonic pattern, and harmonic cancellation by third harmonic injection [76].

2.3.4.2 Closed loop control systems

As opposed to open loop systems, the closed loop techniques incorporate a feedback loop, which senses the required variables under consideration. These systems are more accurate from the point of view of the amount harmonic and reactive power reduction they can achieve. Almost all new techniques in use are of this type. These controllers usually employ digital signal processors (DSPs).

- ***Constant capacitor voltage technique:*** This technique, which is suitable for single and three-phase inverter configurations with a capacitor in the DC link, relies on the fact that the capacitor voltage is the voltage source that controls the current waveform simply by connecting the capacitor to the mains supply through the smoothing inductor. The resulting current is then controlled by

ordinary PWM techniques. Because energy is supplied to or taken from the DC capacitor, the voltage across its terminals fluctuates. To keep this voltage within limits, a reference voltage is chosen. The error difference between the actual capacitor voltage and the reference value determines the active component of power necessary to compensate for capacitor voltage attenuation. This error is added to current controller error signal to determine the overall system error to be processed by the current controller [21-26, 59-65]. This technique is very popular as is clear from the large number of references provided.

- ***Constant inductor current technique:*** This control technique, on the other hand, is suitable for standard converter with inductor in the DC link [19,20,27,43,46]. The operation of the system is then very similar to that of the constant capacitor voltage system when the capacitor voltage is replaced with the inductor current. Although the concept is well established, it is not possible to implement it with present power electronics technology [54].

- ***Optimization techniques:*** The optimization procedure for switched capacitor (SC) and lattice structure circuits is the same [29-33,66]. The rate of rise of the current and the amplitude depend mainly on the size of the capacitors and the initial voltages on them. These factors are function of the switching pattern. The key to controlling these filter configurations is to determine the appropriate switching function for the switches. The main task of the system controller is to minimize a predetermined number of individual load current harmonics, in addition minimizing either the THD or the fundamental component of the filter current. However, this is not performed instantaneously. A time delay exists between the detection of a change in the harmonic current and the application of the new set of switching angles obtained from the optimization procedure. This system is mainly suitable for constant or slowly varying loads.

2.3.5 Classification according current/voltage reference estimation techniques

The reference current/voltage to be processed by the control loops constitutes an important and crucial measure for subdividing active filtering techniques. Figure

2.11 illustrates these estimation techniques, which cannot be considered to belong to the control loop since they perform an independent task by providing it with the required reference for further processing. Most conventional methods of reference estimation can be classified either as time domain or frequency domain. However, other modern techniques exist.

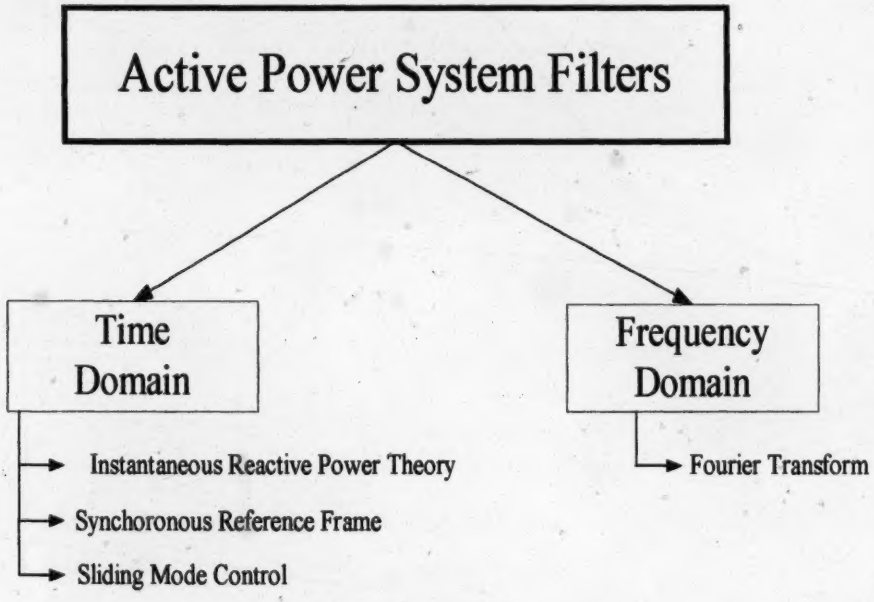


Figure 2.11 Classification of active filters according to current/voltage estimation techniques.

2.3.5.1 Frequency domain approaches

Development of compensating signals in the frequency domain is based on the Fourier analysis of the distorted voltage or current signals to extract compensating commands [27,39,41,77]. Using Fourier transformation, the compensating harmonic components are separated from the harmonic polluted signals and combined to generate compensating commands. However, the on-line application of Fourier transform is a cumbersome computation and results in a large response time.

2.3.5.2 Time domain approaches

Development of compensating signals in the time domain is based on instantaneous derivation of compensating commands in the form of either voltage or current signals from distorted and polluted harmonic voltage or current signals. There is a large number of control methods in the time, which are known as "Instantaneous reactive power theory" [8,42,43,46], "Synchronous d-q reference frame" [69,78,79], "Sliding mode controller" [80,81], etc.

2.4 Conclusions

The review and classifications done in this chapter shows that there has been an increasing concern about power quality and the availability of suitable power switching devices at affordable prices. To facilitate understanding and selection of particular configuration and control techniques for a given application, the classification is based on five main criteria. The power circuit configurations of power conditioners and the ratings of the compensated systems define the two broad categories. The other three classification criteria are based on system parameters to be compensated control techniques employed, and techniques used for estimating reference current/voltage.

It is obvious from the survey that a great deal of work still needs to be done; particularly as the problems associated with generation, transmission, distribution and consumption of power become more serious.

CHAPTER 3

The Proposed Scheme and Standard Control Strategy

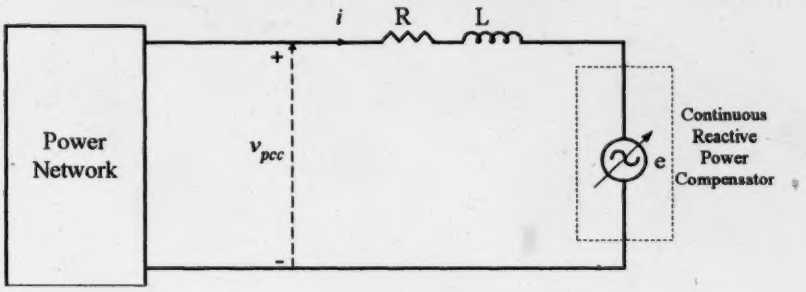
3.1 Introduction

In this chapter an alternative switched capacitor-based power conditioner topology that employs three bi-directional switches and two small capacitors and can be controlled with standard hysteresis current control is proposed. The voltage across the capacitors can be limited to a range of relatively low values by an adequate design of the passive components. A systematic design approach based on a detailed code for simulating currents and voltages in the circuit and a systematic optimization procedure that resulted in graphs that allow the choice of the system components is presented. Simulation results for the scheme when operating as a power quality conditioner will be presented. Finally, the validity of the design will be confirmed with an experimental prototype.

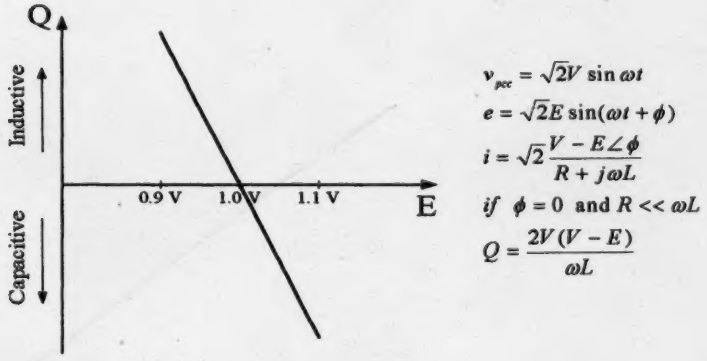
3.2 Principle of Operation of a Switched Capacitor Topology

3.2.1 Basic principle of Continuous Reactive Power Compensation

The economic and technical advantages of continuously adjustable reactive power flow have become evident to electrical engineers since early 1920's [82]. The principle of this method is illustrated in figure 3.1a, where the reactive power flowing from a certain network bus into the feeder, R, L, can be settled to the desired level by adjusting the magnitude and the phase angle of the phasor voltage e=E∠Φ. The principle can be further clarified from the graph shown in figure 3.1b when assuming that the variable voltage source 'e' can be controlled to be in phase with the voltage at the point of common coupling 'v_{pcc}' and as a consequence the reactive power can be made either inductive or capacitive depending only on the magnitude of 'e'.



(a)



(b)

Figure 3.1 The principle of continuous control of KVar.
(a) Equivalent circuit. (b) Reactive power versus control voltage.

Several schemes were proposed to perform this function such as: synchronous condenser [83] and thyristorized static var compensator (SVC) [84]. However, the slow response, special maintenance requirements, and low order harmonics injection are the major limitations of these schemes.

Recent development of semiconductor switches such as insulated gate bipolar transistor (IGBT) has started to open the door for implementation of SVC's with sinusoidal current (Statcom). One of the schemes that have been used to implement this function and presents several advantages in terms of small passive elements and low switching frequency is the switched capacitor power conditioner that will be described in the next section.

3.2.2 Principle of Continuous Reactive Power Compensation with Switched Capacitor (SC)

The simplest known schematic diagram of a "Switched Capacitor Topology" is the one with two bi-directional switches and a single capacitor described in [15] as shown in figure 3.2.

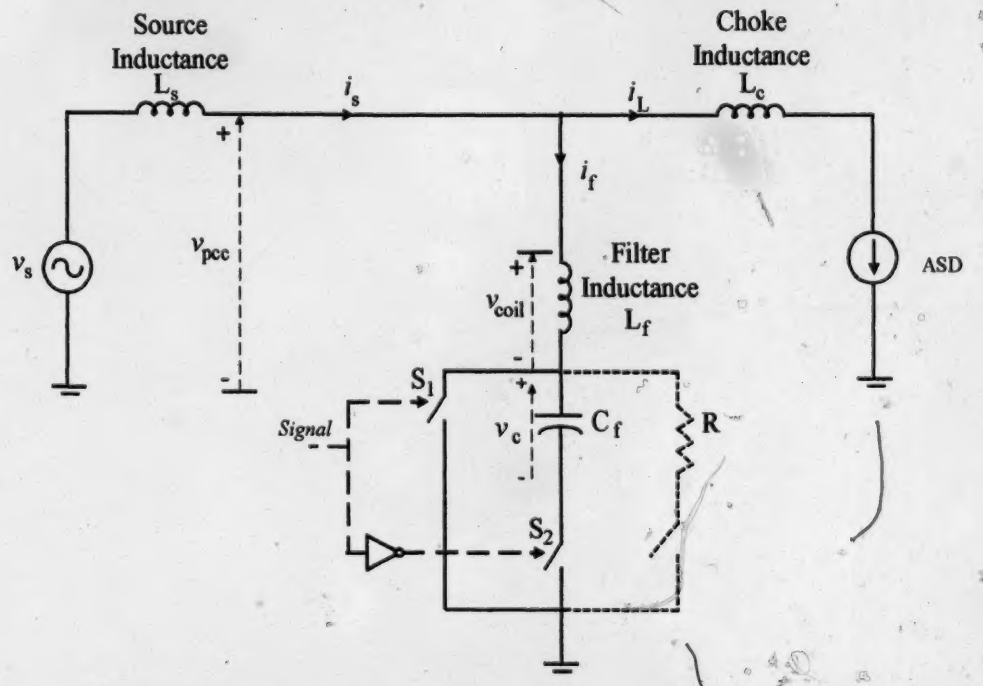


Figure 3.2 Switched capacitor filter with non-linear load.

Ideal waveforms for the voltage at the point of common coupling, v_{pcc}, capacitor voltage, v_c, and SC scheme current (compensating current), i_f, when the SC scheme is working as static var compensator (SVC), are shown in figure 3.3. The current i_f is confined within two closely bound limits, a template, which follows the waveform of any reference current.

Controlling the rate of change of the current in the inductor, which can be made either positive or negative depending on which switch is on, controls the SC scheme current. The coil voltage (v_{coil} = L di/dt) determines the slope of the current. Moreover, at any moment the capacitor voltage should be bigger than the supply voltage, $v_c > |v_{pcc}|$ and should have the same polarity (in phase) to allow the SC scheme to work properly. This condition is easy to achieve due to the inrush current during the starting of the scheme that make the capacitor voltage to be higher than the voltage at the point of common coupling. By virtue of the inductance L_f, the capacitor voltage will charge to a value in excess of the peak of v_{pcc}. This provides an adequate voltage for the SC scheme to begin its operation.

In fact, the magnitude of the rate of change of current in the inductor can be calculated as follows:

$$\frac{di_f}{dt} = \frac{v_{pcc}}{L_f} \quad \& \quad \frac{di_f}{dt} = \frac{v_{pcc} - kv_c}{L_f} \tag{3.1}$$

Where k = 1 if $v_{pcc} > 0$, and k = -1 if $v_{pcc} < 0$.

Therefore, the switches will operate in the following sequence, as shown in figure 3.4:

For the positive cycle of the voltage at the point of common coupling, $v_{pcc}>0$:

- when S_1 is on, S_2 is off, $v_{coil} = v_{pcc}$ and the rate of rise of current has the same polarity of v_{pcc}, di/dt>0.
- when S_1 is off, S_2 is on, the rate of rise of current has the opposite polarity of v_{pcc} since, $v_c > | v_{pcc} |$, di/dt<0.

For the negative cycle of the of voltage at the point of common coupling, $v_{pcc}<0$:

- when S_1 is on, S_2 is off, $v_{coil} = v_{pcc}$ and the rate of rise of current has the same polarity of v_{pcc}, di/dt<0.

- when S_1 is off, S_2 is on, the rate of rise of current has the opposite polarity of v_{pcc} since, $v_c > |v_{pcc}|$, di/dt>0.

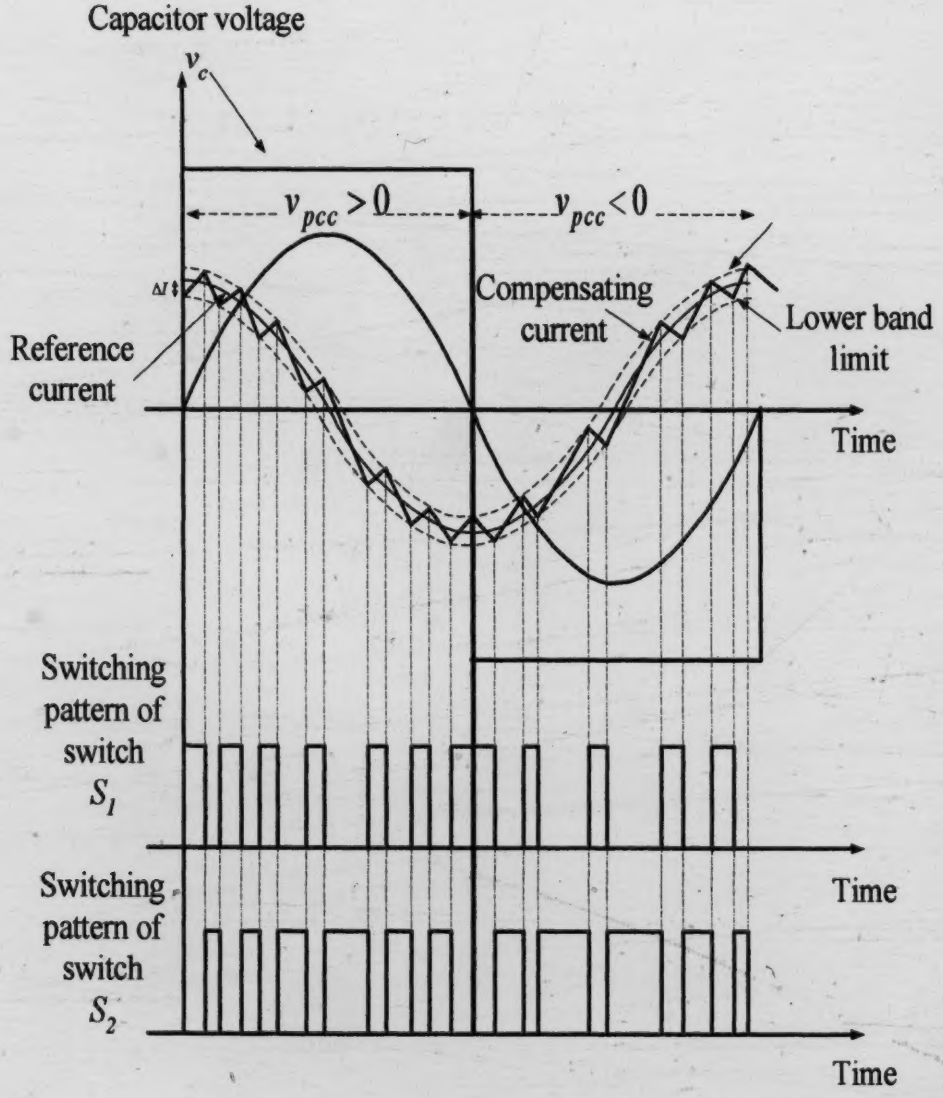
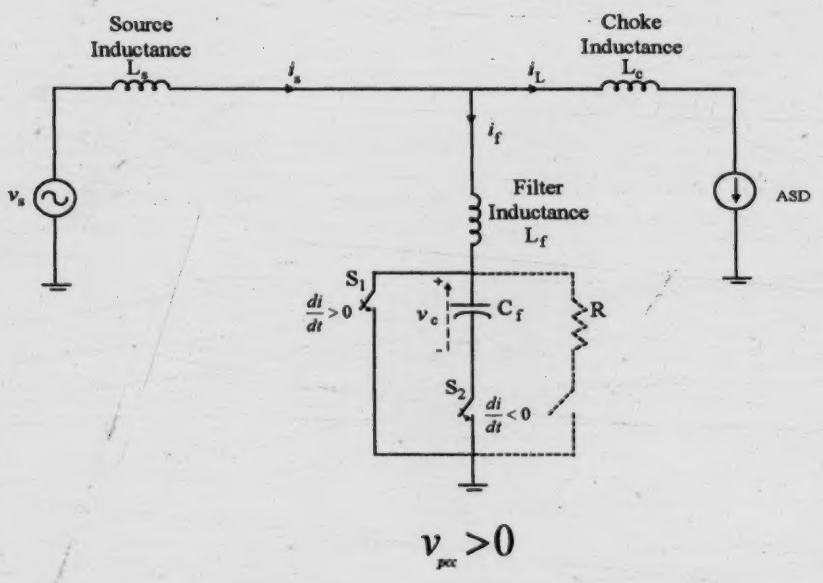


Figure 3.3 Standard hysteresis control.



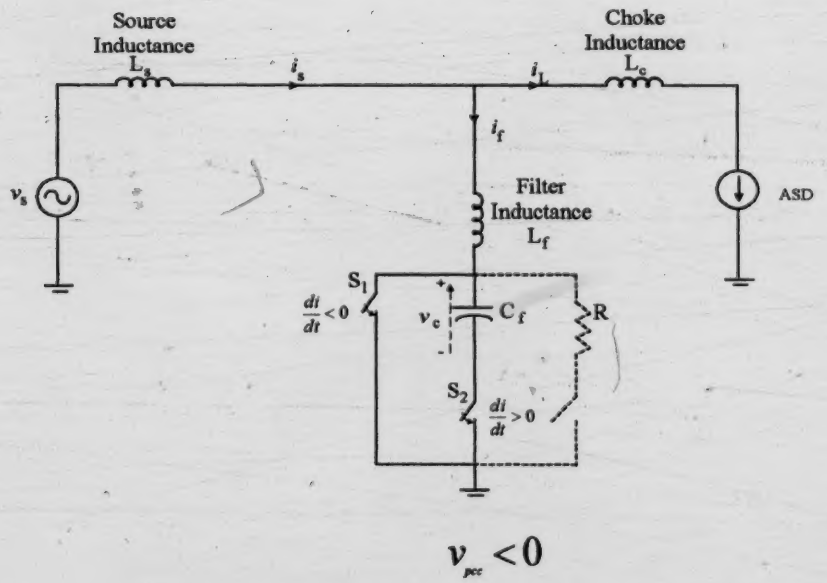


Figure 3.4 Different modes of operations for SC circuit.

However, when the standard hysteresis current control, shown in figure 3.3, is employed, there will be an unexpected phase shift between the source and the capacitor waveforms, as seen in figure 3.5. This happens due to the inertia of the capacitor that doesn't allow the capacitor to flip its polarity instantaneously. The control strategy should be counted for this shift, adding more complications to the design. Therefore, the control scheme used in [15] is based on optimization techniques for the generation of gating signals. Further, the computation of the optimization process takes a long time that makes this technique unsuitable for online control. Further, for the experimental set-up, a third branch with a switch and a resistor is included, which probably help to speed up the discharge of the capacitor, thus reducing the phase shift between v_{pcc} and v_c but adding more losses to the circuit.

Different other alternatives for the previous scheme, as shown in figure 3.6, had been proposed to improve the filter performance [13,16-18]. However, these schemes required additional switches or passive elements than the previous scheme, which means more switching losses and additional complication to the control strategy.

In conclusion, to improve the performance of the switched capacitor topology we have to do the following:

a- avoiding any time delay between the zero crossings of both the capacitor voltage and voltage at the point of common coupling,

b- improving control strategy to make it suitable for online control,

c- reducing the number of switching devices or passive components to reduce the scheme cost.

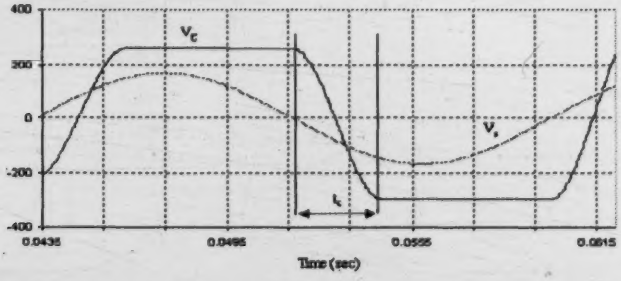
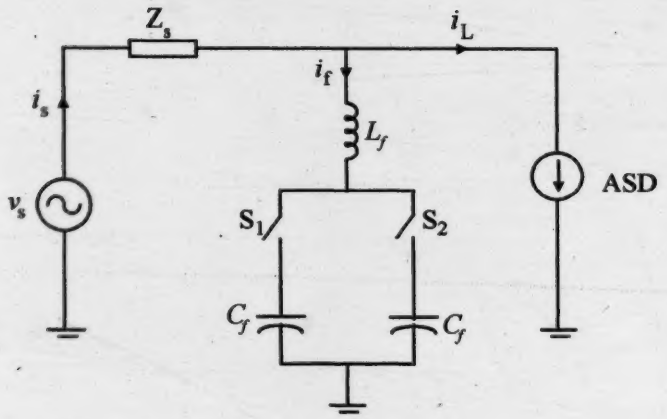
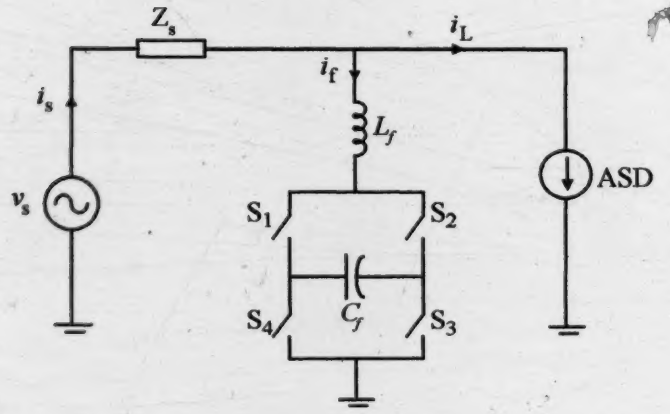


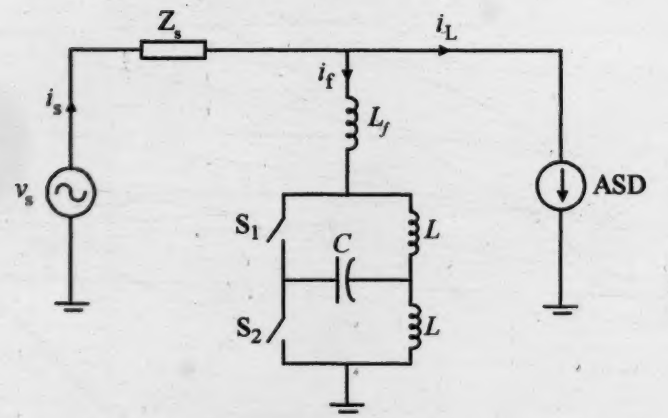
Figure 3.5 Voltage at the point of common coupling and capacitor voltage waveforms.



(a)



(b)



(c)

Figure 3.6 Switched capacitor configurations.

3.3 The Proposed Scheme

3.3.1 Power Structure and Standard Control Strategy

The schematic diagram of the proposed topology is shown in figure3.7 [68]. It employs two switched capacitors which present voltage waveforms that are mostly dc with inverse polarities. In the basic operating mode, shown in figure 3.7, switches S_1 and S_2 operate complementarily to control the rate of rise of current in the positive semi cycle ($v_{C2} > +v_{pcc\_peak}$), up and down respectively. For the negative semi cycle, S_1 and S_3 operate complementarily, where $v_{C3} < -v_{pcc\_peak}$, resulting in a fall and rise of the inductor current respectively. This way the inductor current is made to follow a command current template in a hysteresis mode. The schematic diagram of the circuit that implements this logic is shown in figure 3.8. The error (δ) between the actual (i_f) and the command current (i_c) is calculated and fed to a hysteresis comparator and a logic circuit that yields the desired gating signals for S_1, S_2 and S_3. From the discussion given above, the logic circuits in figure 3.8 can be designed using the truth table for each switch as follows:

- For S_2:

	v_{pcc} ($v_{pcc}>0$)
δ ($\delta>0$)	1
$\bar{\delta}$ ($\delta<0$)	0

$$S_2 = v_{pcc} \bullet \delta$$

- For S_3:

	$\overline{v_{pcc}}$ ($v_{pcc}<0$)
δ ($\delta>0$)	0
$\bar{\delta}$ ($\delta<0$)	1

$$S_3 = \overline{v_{pcc}} \bullet \bar{\delta}$$

- Finally, for the logic of S_1, it can be deduced from the logic of both S_2 and S_3, as it is complementary of any one of them. Therefore, the logic of S_1 is:

$$S_1 = \overline{(S_2 + S_3)} = \overline{\left(v_{pcc} \bullet \delta + \overline{v_{pcc}} \bullet \bar{\delta}\right)}$$

By employing two capacitors we could achieve the following:

- there is no need for changing the polarity of the capacitor voltage in synchronism with v_{pcc},
- standard hysteresis current control can be used.
- due to the simplicity of the control circuit, the scheme can be used for online control as the delay time is very small.

This way the proposed scheme could improve most of deficiencies associated with the original topology.

Finally, for proper operation of the proposed SC scheme, the capacitor voltage magnitudes should always be larger than the peak voltage of the ac mains. Passive elements, L_f and C_f, command current, i_c, and initial capacitor voltage, V_{C0}, are the main factors that affect the capacitor voltages. Therefore, for a known command current, there is a need for an adequate choice of the passive components that is rather complicated due to the L-C interaction and needs an optimization procedure to select them as will be shown in the next section.

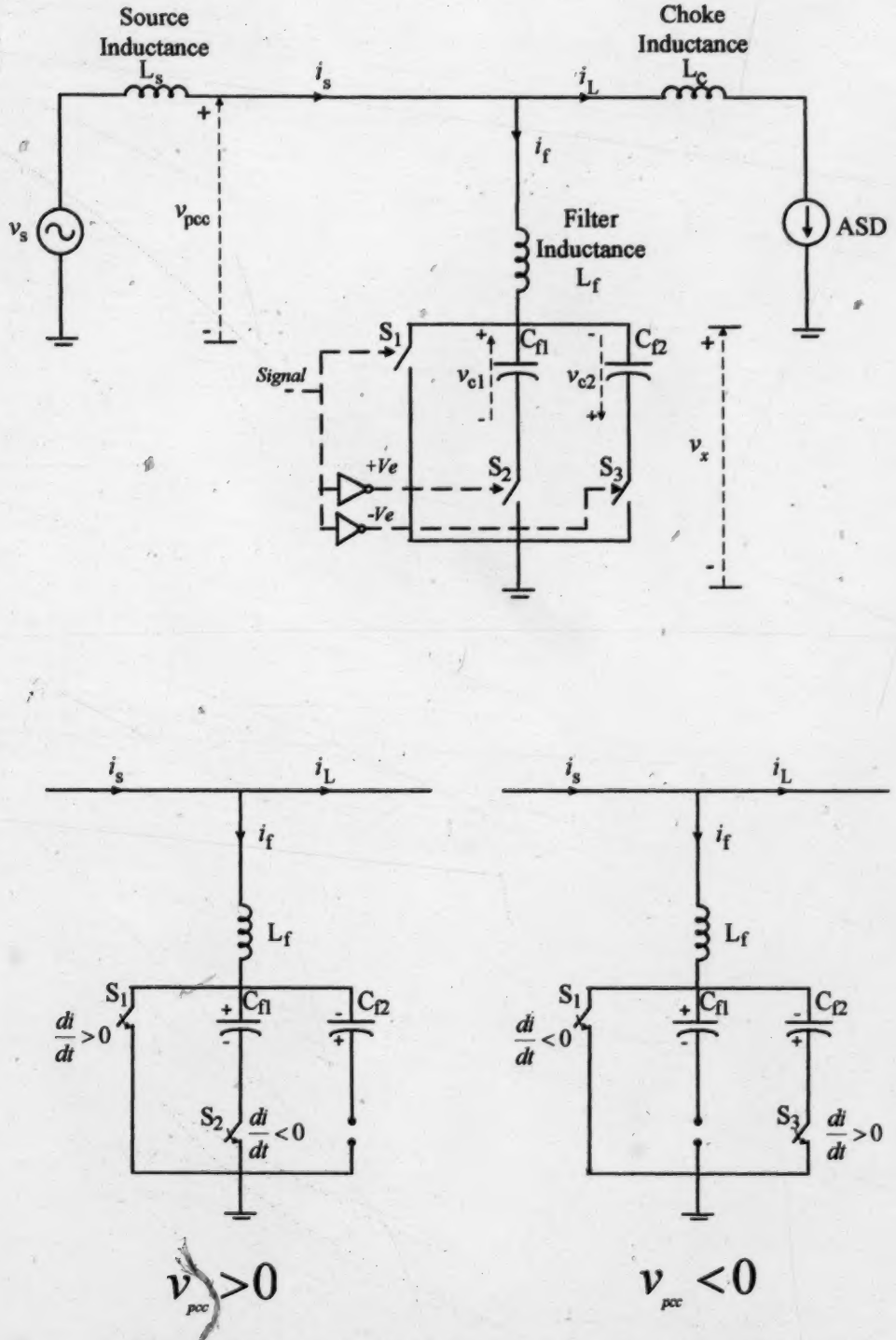


Figure 3.7 Proposed switched capacitor based power conditioner.

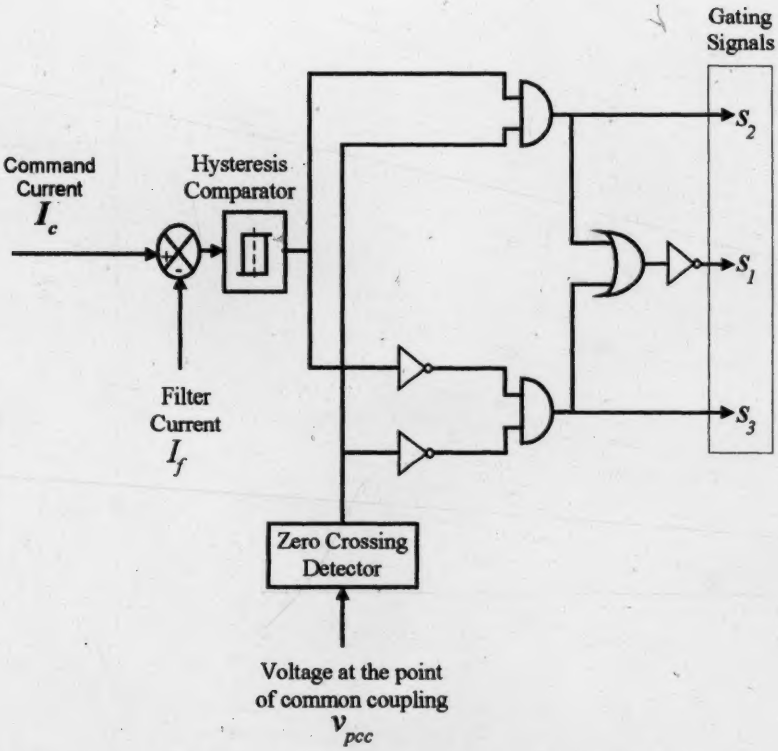


Figure 3.8 Control circuit of the standard switching strategy.

3.3.2 Designing the Proposed Topology

3.3.2.1 Generic considerations.

The choice of the passive elements should consider some basic aspects of the topology. The reactor, should be selected so that the rate of change of the current satisfies the following conditions:

$$\left|\frac{di_f}{dt}\right| > \left|\frac{di_{compensation}}{dt}\right| \tag{3.2}$$

From (3.3) one sees that high rates of rise of current can be achieved by using small inductors. However, with controlling the SC scheme with hysteresis current control, as the supply voltage increases, the rate of rise becomes bigger as well as the switching frequency.

$$L_f < \left|\frac{v_{coil}}{\frac{di_{compensation}}{dt}}\right| \tag{3.3}$$

Regarding the choice of the capacitor, it should be made as small as possible, for reduced cost, but big enough to limit the voltage ripple (ΔVc_{max}) to an acceptable value. Further, for a known initial capacitor voltage and reference current, the capacitor should be designed so that its voltage is always bigger than the voltage at the point of common coupling for proper operation of the SC scheme. An initial guess of the value of the capacitor, for the optimization procedure described in the following section is:

$$C_f > \frac{\max\left|\int_0^t i_f(t)\,dt\right|}{\Delta V_c\big|_{max}} \tag{3.4}$$

Where $i_f(t)$ is the instantaneous filter current during the conduction period of S_2 and S_3.

3.3.2.2 *Deriving Design Equations*

The scheme can be split into two different modes as shown in figure 3.9. This figure can be used to obtain representative equations that describe the operation of the filter current at capacitor voltage at all points within each switching period.

The general expression for the current during any time interval (*k*), is as follows:

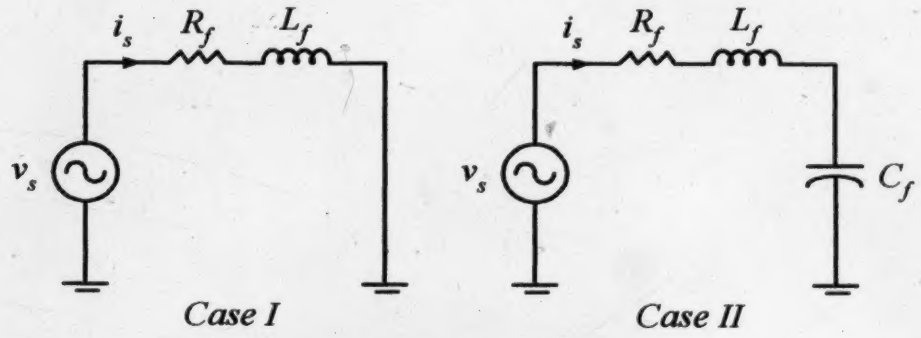
$$i_{f_K} = i_{forced\ K} + i_{natural\ K} \tag{3.5}$$

where:

i_{f_K} is the magnitude of the total filter current at any instant of time k,

$i_{forced\ K}$ is the magnitude of the forced filter current at any instant of time k,

$i_{natural\ K}$ is the magnitude of the natural filter current at any instant of time k.



R_f is the SC scheme resistance

L_f is the SC scheme inductance

C_f is the SC scheme capacitance

Figure 3.9 Circuit separation

- Case *I*:

$$Z^{I}(s) = R_f + sL_f \tag{3.6}$$

where the single root is

$$s^I = \alpha^I = \frac{R_f}{L_f}$$

Hence

$$i^I_{forecd\ \kappa}(t) = \frac{V_m}{\sqrt{R_f^2 + (\omega L_f)^2}} \sin\left[\omega t - \tan^{-1}\left(\frac{\omega L_f}{R_f}\right)\right] \quad (3.7)$$

and

$$i^I_{natural\ \kappa}(t) = B^I_k\ e^{-\alpha^I t} \quad (3.8)$$

Solving for B^I_k using initial conditions $i^I_{f_K}(t_{k-1})$, $i^I_{forced_K}(t_{k-1})$, and t_{k-1} for Case *I* during the time interval *k* is:

$$B^I_k = \frac{i^I_{f_K}(t_{k-1}) - i^I_{forced\ \kappa}(t_{k-1})}{e^{-\alpha^I t_{k-1}}} \quad (3.9)$$

where

Finally, from Eq.(3.5), Eq.(3.7), Eq.(3.8), and Eq.(3.9), the current $i^I_{f_K}(t)$ for Case I during the time interval *k* is:

$$i^I_{f_K}(t) = G_I \sin(\omega t - \gamma_I) + B^I_k\ e^{-\alpha^I t} \quad (3.10)$$

where

$$G_I = \frac{V_m}{\sqrt{R_f^2 + (\omega L_f)^2}}$$

$$\gamma_I = \tan^{-1}\left(\frac{\omega L_f}{R_f}\right)$$

Finally, the capacitor voltage in this case is constant and equal to the final capacitor voltage from case *II* as follows:

$$v^I_{C_K}(t_k) = v^{II}_{C_K}(t_{k-1}) = V_{0_{k-1}} \quad (3.11)$$

Eq. (3.10) and Eq. (3.11) can then be used to determine the filter current and capacitor voltage during the time interval *k* while the circuit remains in this

state. At each switching transition the initial conditions change. Therefore the preliminary calculations must be reevaluated.

- ***Case II:***

The total impedance of the circuit in Case *II* is:

$$Z^{II}(s) = R_f + sL_f + \frac{1}{sC_f} \qquad (3.12)$$

The previous equation has two roots that are:

$$s_1^{II} = -\alpha^{II} + \sqrt{\alpha^{II^2} - \omega_0^2}$$

$$s_2^{II} = -\alpha^{II} - \sqrt{\alpha^{II^2} - \omega_0^2}$$

where

$$\alpha^{II} = \frac{R_f}{2L_f} \;\&\; \omega_0 = \frac{1}{\sqrt{L_f C_f}}$$

If the value of R_f is too small such that $R_f << \omega L_f$, this means that $\alpha^{II^2} << \omega_0^2$ and the response is under damped, and therefore the general solution of the equation is:

$$i_{f_K}^{II}(t) = i_{forecd_K}^{II}(t) + e^{-\alpha^{II}t}\left(A_{1k}\cos|\beta|t + A_{2k}\sin|\beta|t\right) \qquad (3.13)$$

where

$\beta = \sqrt{\omega_0^2 - \alpha^{II^2}}$

A_{1k} & A_{2k} = constants

The forced current can be calculated by:

$$i_{forecd_K}^{II}(t) = \frac{V_m}{\sqrt{R_f^2 + \left(\frac{\omega^2 L_f C_f - 1}{\omega C_f}\right)^2}} \sin\left[\omega t - \tan^{-1}\left(\frac{\omega^2 L_f C_f - 1}{\omega C_f R_f}\right)\right]$$

(3.14)

From Eq.(3.5), (3.13), and (3.14), the current $i_{f_k}^{II}(t)$ during the time interval *k* is:

$$i_{f_k}^{II}(t) = G_{II}\ \sin(\omega t - \gamma_{II}) + e^{-\alpha^{II} t}\left(A_{1k}\ \cos|\beta|t + A_{2k}\ \sin|\beta|t\right) \qquad (3.15)$$

where

$$G_{II} = \frac{V_m}{\sqrt{R_f^2 + \left(\frac{\omega^2 L_f C_f - 1}{\omega C_f}\right)^2}}$$

$$\gamma_{II} = \tan^{-1}\left(\frac{\omega^2 L_f C_f - 1}{\omega C_f R_f}\right)$$

A_{1k} & A_{2k} should be recalculated at the end of each switching transition to be used as the initial conditions for the next state.

Finally, the capacitor voltage in case *II* can be given as:

$$v_{C_k}^{II}(t_k) = \frac{1}{C_f}\int_{t_{k-1}}^{t_k} i_{f_k}^{II}(t_k)\,dt + V_{0_{k-1}} \qquad (3.16)$$

3.3.2.3 Calculating Circuit Components

Eq. (3.10), (3.11), (3.15) and (3.16) can be used to obtain the SC scheme current and capacitor voltage waveforms at all switching instants. These are obtained from the control circuit shown in figure 3.8, for a given hysteresis window (ΔI), usually 5%. The results are then used to evaluate the performance of the scheme in terms of the THD of the source current (i_s) and calculate the average switching frequency. Then the values of L_f and C_f are changed according to the algorithm of the flow chart of figure 3.10 and the simulation process is repeated. From a practical point of view, an inductor value $L_f < 5\%$ of the scheme base impedance will enable a low and cost effective scheme with acceptable performance in terms of switching frequency and total harmonic distortion (THD) [85,86].

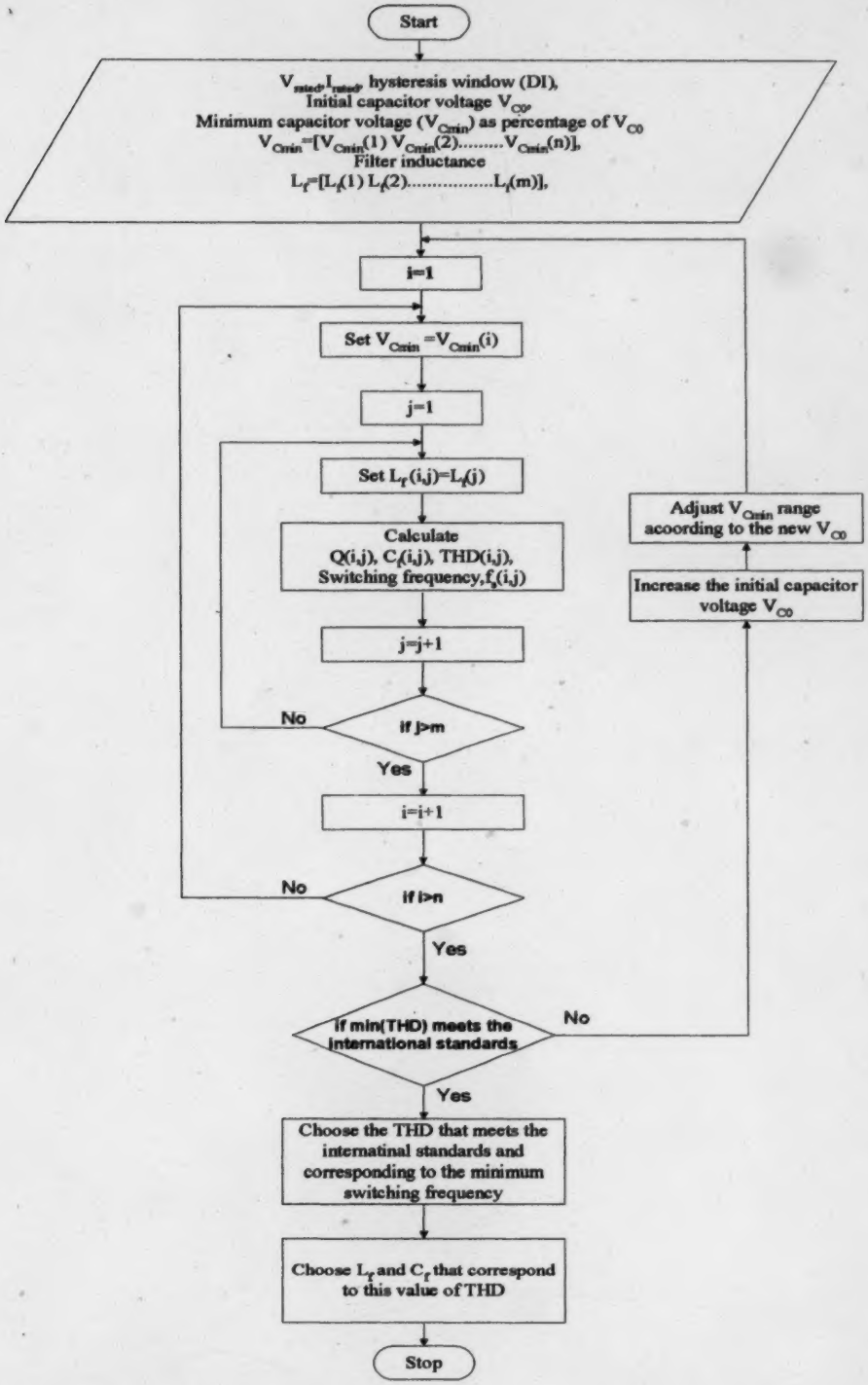


Figure 3.10 Optimization procedure for selection of different filter parameters.

The determination of the capacitor value is less straightforward than the filter inductor, as it depends on the initial, minimum, and maximum capacitor voltages (V_{C0}, V_{Cmin}, V_{Cmax}). On the one hand, V_{Cmin} should be greater than the peak of the v_{pcc} for proper operation of the filter. On the other hand, V_{Cmax} should be limited to a relatively small voltage to decrease the switch ratings. A closed form for calculating V_{C0}, V_{Cmin}, V_{Cmax} requires a precise knowledge of the capacitor current. This has been done for a similar topology operating as a Static Var Compensator in [1]. Assuming that v_{pcc} can be represented as follows:

$$v_{pcc}(t) = \sqrt{2}V \sin \omega t \tag{3.17}$$

and the filter current, that is assumed to be reactive as a first assumption, is:

$$i_f(t) = \pm\sqrt{2}I_f \cos \omega t \tag{3.18}$$

and from the power balance in the scheme:

$$p_f = v_{pcc} i_f = L_f \frac{di_f}{dt} i_f + v_c C_f \frac{dv_c}{dt} \tag{3.19}$$

substituting form Eq. (3.19) and (3.20) in Eq. (3.21) gives

$$\pm Q \sin 2\omega t = -XI_f^2 \sin 2\omega t + Cv_c \frac{dv_c}{dt} \tag{3.20}$$

integration of the above equation results in

$$v_c^2(t) = -\frac{XI_f^2 \pm Q}{C\omega} \cos 2\omega t + K \tag{3.21}$$

where K is the integration constant. Keeping in mind that at t=0; $v_c = V_{C0}$, results in

$$v_c(t) = \sqrt{V_{C0}^2 + \frac{XI_f^2 \pm Q}{\omega C}(1 - \cos 2\omega t)} \tag{3.22}$$

where

$Q_f = VI_f$ is the required reactive power from the SVC

I_f is RMS value of the SVC current

From Eq. (3.22) the capacitor maximum voltage V_{Cmax} (during capacitive current) or minimum voltage V_{Cmin} (during inductive current) can be calculated and it will always occur at $\omega t = \pi/2$. By selecting V_{C0} to be at a certain level

bigger than the peak of the voltage at the point of common coupling, and for different values of capacitor voltage ripples, the capacitor value can be calculated. Then, the optimization technique is performed to provide a set of graphs for THD, switching frequency, and capacitor value, for different inductor values that will allow the choice of optimum values for L_f & C_f.

3.4 Reactive Power Compensation with the Proposed SC Scheme

This section presents the analysis and design procedure of the SC based power converter when used for reactive power control. Control circuits for generating the reference current is described. Finally, simulation results for steady state operation are carried out to analyze the performance of the scheme under different loading conditions.

3.4.1 Generation of the Reference Current for the Proposed Control Strategy

3.4.1.1 General Consideration

The hysteresis current control scheme presents several desirable features such as easy implementation and fast and accurate response. However, since the compensator does not include large storage elements, the net active power flow in the compensator should be minimum in steady state to maintain the capacitor voltages at the required level.

An investigation of the existing control strategies for power conditioners has been done to select one that meet the requirements of the SC scheme and can be easily implemented for reactive power compensation. Instantaneous Reactive Power Theory (IRP) [87], Frequency Domain Analysis [88], and d-q Reference Frame Theory are commonly used but they have the inherent disadvantages that they are complex to implement, difficult to adjust, or have relatively long delay times. Moreover, since dynamic compensation requires rapid detection of the required signal, a control circuit that is based on analog components is better than digital detection that is not as fast [89,90]. Therefore, a detection technique

that is based on Adaptive Noise Canceling (ANC) is chosen for generating the reference current for compensating reactive currents for a given load [91,92]. A detail of the technique is given below.

3.4.1.2 Principle of operation of Adaptive Noise Canceling (ANC) Technique

The Adaptive Noise Canceling technique has been widely used in recent years [91]. It can maintain the system in the best operating state by continuously self-studying and self-adjusting from start to end. The basic noise-canceling situation is illustrated in figure 3.11. A signal is transmitted over a channel to a sensor that receives the signal, s, plus an uncorrelated noise, n_0. The combined signal and noise, $s+ n_0$, forms the "primary input" to the canceller. A second sensor receives a noise n_1, which is uncorrelated with the signal but correlated in the same unknown way with the noise n_0. This sensor provides the "reference input" to the canceller. The noise n_1 is filtered to produce an output y, which is an approximate replica of n_0. This output is subtracted from the primary input $s+ n_0$ to form the system output, $s+ n_0-y$.

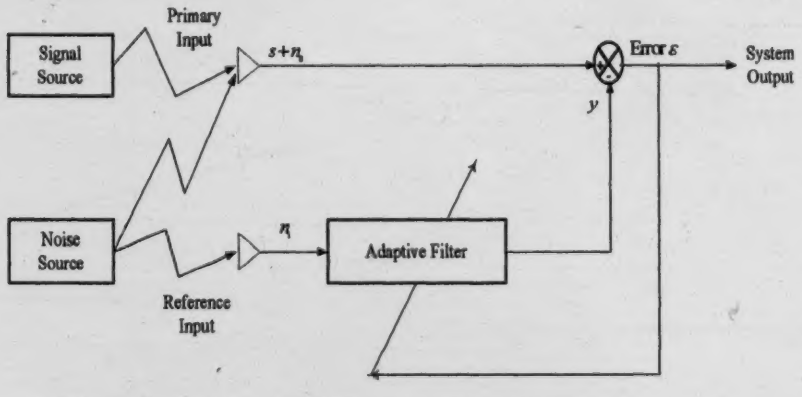


Figure 3.11 Adaptive noise canceling concept.

In the system shown in figure 3.11, the reference input is processed by an adaptive filter, which automatically adjusts its own response through a least-

squares algorithm. Thus the filter can operate under changing conditions and can readjust itself continuously to minimize the error signal ε. An ideal situation is when the same noise in the primary input as in the reference input is completely eliminated and the system output contains only the signal components as those contained in the reference input.

Generally speaking, the active component of the fundamental load current and the ac source voltage are in phase but with different amplitudes. If the fundamental voltage acts as the reference input and the load current as the primary input, it is similar to the foregoing situation that the reference input is processed by an adaptive filter to produce an output, which equals the active component of the primary input in amplitude and phase. This output is subtracted from the primary input to cancel its active component; consequently the system output will be the sum of the harmonic and reactive components.

3.4.1.3 Reference Current Generation Using Adaptive Noise Canceling (ANC) Technique

The schematic diagram for the circuit that performs the function of the adaptive ANC technique is shown in figure 3.12.

Under normal circumstances, the utility can be assumed to be a sinusoidal voltage source.

$$v_s(t) = V_m \sin \omega t \tag{3.23}$$

If a load is applied, i_L (t) can be expressed as the sum of a fundamental current, i_{L1} (t), and harmonic current, i_{Lh} (t). The fundamental current can be further decomposed into an active current component $i_{Lp}(t)$ and reactive current component $i_{Lq}(t)$.

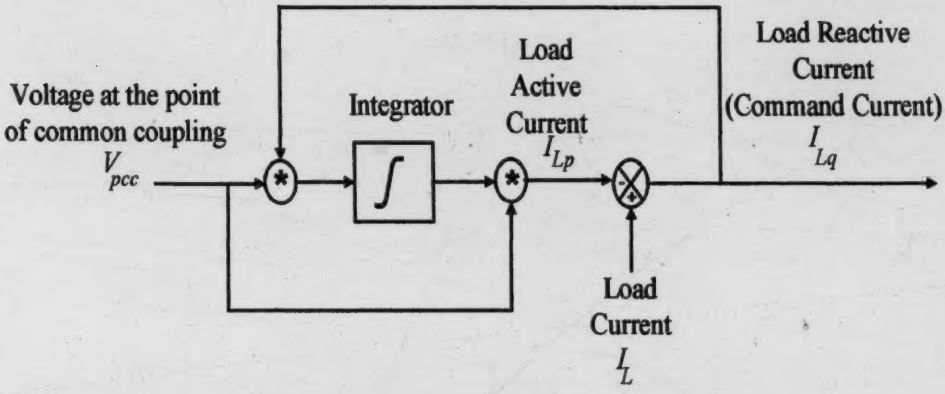


Figure 3.12 Scheme for generating the reference current of the power conditioner.

$$i_L(t) = I_1 \sin(\omega t + \theta_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \theta_n)$$
$$i_L(t) = i_{L1}(t) + i_{Lh}(t) \tag{3.24}$$

where

$$i_{L1}(t) = I_1 \sin(\omega t + \theta_1) = i_{Lp}(t) + i_{Lq}(t)$$
$$i_{Lp}(t) = I_1 \cos\theta_1 \sin\omega t,$$
$$i_{Lq}(t) = I_1 \sin\theta_1 \cos\omega t,$$
$$i_{Lh}(t) = \sum_{n=2}^{\infty} I_n \sin(n\omega t + \theta_n)$$

Therefore, the load power can be expressed as:

$$\begin{aligned} p_L(t) &= v_s(t) i_L(t) \\ &= I_1 V_m \sin^2 \omega t \cos\theta_1 + I_1 V_m \sin\omega t \cos\omega t \sin\theta_1 \\ &\quad + \sum_{2}^{\infty} V_m \sin\omega t I_n \sin(n\omega t + \theta_n) \end{aligned} \tag{3.25}$$

By integrating Eq. (3.25) over a whole period, the average power can be calculated as:

$$
\begin{aligned}
p_{Lav} &= \frac{1}{T}\int_0^T p_L(t)dt \\
&= \frac{1}{\omega T}\int_0^{\omega T}(I_1 V_m \sin^2 \omega T \cos\theta_1)d\omega t + \\
&\quad \frac{1}{\omega T}\int_0^{\omega T}(I_1 V_m \sin \omega T \cos \omega T \sin\theta_1)d\omega t + \\
&\quad \frac{1}{\omega T}\int_0^{\omega T}(V_m \sin \omega T \sum_{n=2} I_n \sin(n\omega T + \theta_n))d\omega t
\end{aligned}
\tag{3.26}
$$

By applying the Orthogonal Function theory [92] on the above integration, the second and third terms in the right hand side of Eq. (3.26) will be equal to zero. Therefore, the final output of the integration process will be:

$$p_{Lav} = V_m I_1 \cos\theta_1 \tag{3.27}$$

Comparing Eq. (3.27) with Eq. (3.24), one can see that the value of p_{Lav}, is equal to the peak value of the fundamental active current, i_{Lp} when it is scaled by a factor equal of V_m, which is done automatically by the adaptive filter.

Finally, the load active current component, i_{Lp}, is subtracted from the load, i_L, current to get the final current command to the filter, i_c.

Therefore, the SC scheme should provide the following compensation current

$$
\begin{aligned}
i_c(t) &= i_L(t) - i_{Lp}(t) \\
&= i_{Lq}(t) + i_{Lh}(t)
\end{aligned}
\tag{3.28}
$$

The system will reach its steady state when the integrator output is constant which means that $i_{Lp}(t)$ is in phase with $v_{pcc}(t)$. Finally, the final current command, i_c(t), to the SC scheme is compared with the actual current, $i_f(t)$, and the error is passed through a hysteresis window and a logic circuit that yields the desired gating signals for S_1, S_2 and S_3.

3.4.2 Design Procedure

3.4.2.1Estimation of the Average Switching Frequency

The hysteresis current controller ideally has a constant current ripple, ΔI, but no defined switching period, Δt [93].

The average switching frequency (ASF) of the scheme can be calculated as follows:

$$ASF = \frac{N_s}{T} \tag{3.29}$$

where

N_s = number of switching per line period

T = Fundamental period

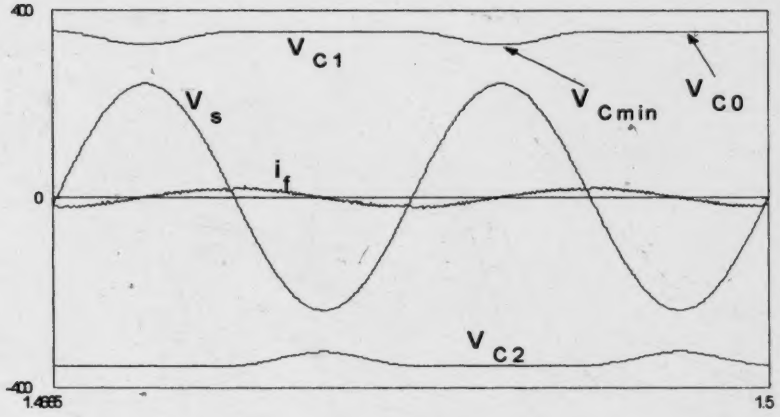
3.4.2.2 Optimization Procedure and Design Example

The optimization procedure is based on a mathematical model that has been presented in Section 3.3.2. The model describes the state of the scheme, in terms of the current and capacitor voltage, at any instant of operation. The waveforms, such as those presented in figure 3.13, are a result of this code. The inputs for the optimization procedure are:

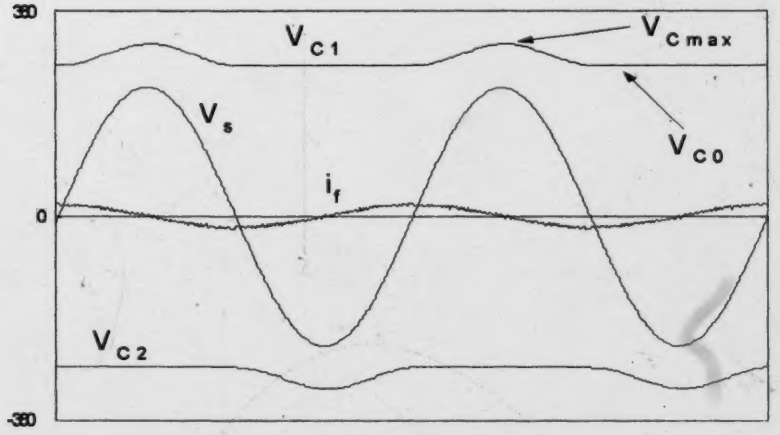
1- rated voltage (120 V),
2- rated current for the power conditioner operating as SVC (5 A),
3- hysteresis window as 5% of the peak rated current (0.35 A),
4- minimum allowable capacitor voltage $V_{Cmin} = 1.1V_{pcc} = 187$ V.
5- minimum initial desired capacitor voltage, $(V_{C0})_{min}$, is designed to allow a maximum of 20 % in the capacitor voltage ripple in order to reduce the size of the capacitor and switches ratings.

$$V_{C0})_{min} = 187/0.8 \approx 235 \text{ V}$$

This is the boundary of the initial capacitor voltage that will allow the SC scheme to work properly up to 20% ripple in the capacitor voltage. On the one hand, if the steady state of the initial capacitor voltage dips below this value, the SC scheme performance will deteriorate.



(a)



(b)

Figure 3.13 Typical waveforms for the supply voltage v_{PCC}, capacitor voltages, v_{c1} & v_{c2} and the power conditioner's current i_f for

a- Reactive power absorption.

b- Reactive power generation.

On the other hand, if the initial capacitor voltage exceeds this limit, the SC scheme will work properly but the passive components and switches should have higher ratings. Therefore, the mathematical model will have a great role in checking the feasibility of scheme, predicting and designing the SC scheme components for different loading conditions.

6- vectors with prospective values for V_{Cmin} as percentage of the initial voltage, the difference between V_{C0} and V_{Cmin} will represent the ripple in the capacitor voltage

   a. ΔV_{C1}= 10%, V_{Cmin1}=0.90*235≈212 V

   b. ΔV_{C2}= 15%, V_{Cmin2}=0.85*235≈200 V

   c. ΔV_{C3}= 20%, V_{Cmin3}=0.80*235≈188 V

7- L_f varies from 2% to 8% of the SC scheme rating.

L_f=[0.0013 0.0019 0.0025 0.0030 0.0036 0.0042 0.0048]H.

An initial guess for the capacitor is calculated and the code runs a simulation until the steady state is reached. For example, if L_f= 0.0013, and ΔV_{C1}=10%, using (3.24) the capacitor can be calculated to be: C_f=350 uF.

The mathematical code will input the above data and based on the current and voltage waveforms the code calculates the THD of the SVC current, the average switching frequency and the actual minimum capacitor voltage. Then the values of L_f and C_f are changed according to the algorithm of the flow chart of figure 3.10 and the simulation process is repeated automatically.

Figure 3.14a shows the calculated values of the THD of the source current, i_s, for different values of inductor, and for three voltage ripple values in the capacitor, 10%, 15%, and 20% that are shown as ΔV_{C1}, ΔV_{C2} and ΔV_{C3} respectively, measured from the initial capacitor voltage. The figure reveals that the smaller the voltage ripples the lower the THD. This happens because the difference in the capacitor voltage and the voltage at the point of common coupling becomes bigger and according to (3.1), this makes the rate of rise of current (di/dt) faster. Further, the smaller the filter inductor, the smaller the THD. This happens due to the effect of the inductor value on di/dt. For large

inductors, the rate of rise of the current, di/dt, becomes slow and the command current will not be able to fast track the required reference current that add some distortion to supply current waveform.

The effect of the inductor size on the switching frequency is also shown in Figure 3.14b. The maximum average switching frequency lies between 1.7 and 4.6 kHz, which ensures that the switching losses are small and the system doesn't need big cooling requirements.

Finally, figure 3.14c presents the change of the required capacitor for various inductor sizes and different capacitor voltage ripples. However, there is no considerable change in the value of the capacitance with respect to the inductor value.

By investigating the figures, for a supply voltage of 120 V and a capacitive load of C_{load} = 300 uF and R_{load} = 10 Ω, one can choose an inductor L_f = 3.0 mH (5%) and capacitor C_f = 260 uF (190%) that will result in a THD of 2.2% and a switching frequency of 2.1 kHz. Further, the capacitors will have an absolute minimum voltage V_{Cmin} of 235V, and an initial voltage V_{C0} of 265V.

From the above voltages, the voltage that should be supported by each switch should be twice as high = 530V. The available IGBTs in the market have the rating of 600V. Therefore, the switches will be selected to be 600V and 15 A for safety operations. Finally, from the above analysis, it can be concluded that:

- When the capacitor voltage is uncontrolled, the calculation of the passive components will be valid if and only if the start up voltage will exceed a certain boundary limit.
- Using the mathematical model can verify the feasibility of the design.
- The value of the start up voltage depends on the values of the passive elements that may change with different loads.
- Controlling the capacitor start up voltage by adding additional control circuit or adding a voltage regulation loop will be beneficial in fixing the capacitor voltage at certain required limit.

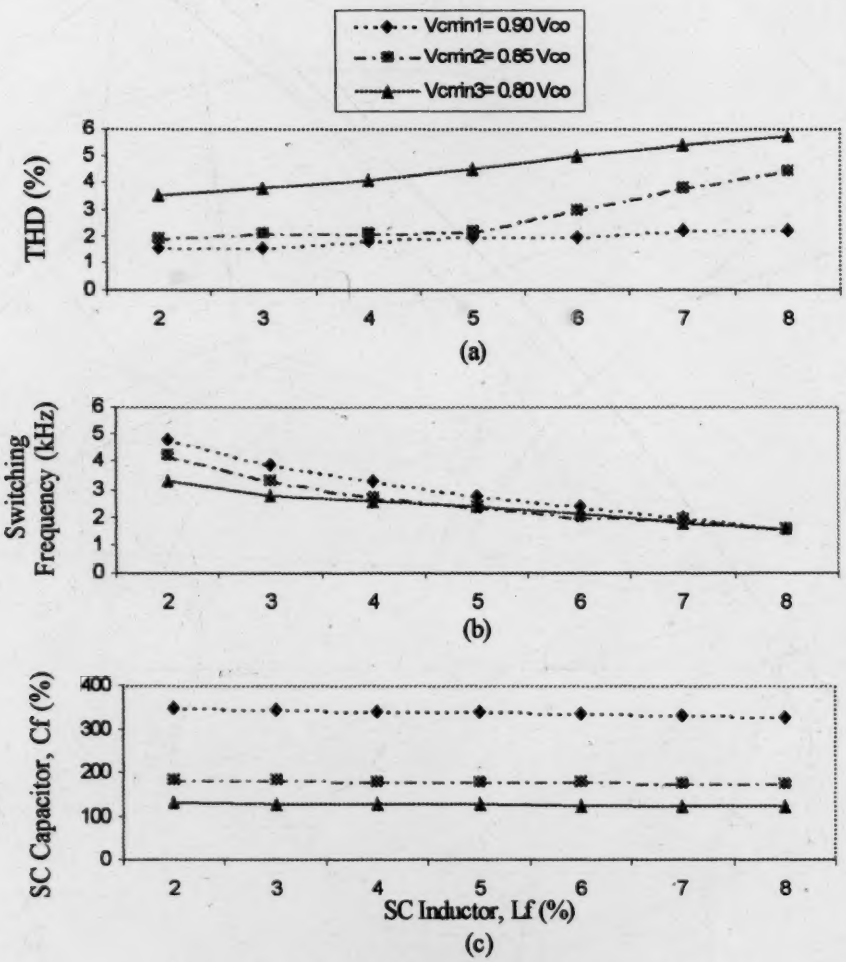


Figure 3.14 Optimization procedure results.

3.5 Simulation Results

The validity of the design procedure is verified by means of simulation, with PSCAD. The overall performance of the proposed power conditioner is evaluated in the next section with a laboratory prototype.

The case study is the same one used for describing the design procedure in the previous section: a SVC generating reactive power, and as shown in figure 3.15. Further, a non-linear load consisting of a diode bridge rectifier with a capacitive filter is simulated to investigate the effectiveness of the power conditioner for harmonic mitigation. The system parameters used in the simulation are as follows:

- Utility system: Single-phase ac supply of 120 Vrms, 60 Hz; Line resistance, $R_s = 0.1\ \Omega$, Line inductance, $L_s = 0.1$ mH
- SC VAR compensator: $L_f = 3.0$ mH, $C_f = 260.0\ \mu$F;
- Load:
  - Linear Load:
    (a) Inductive load: L= 24.0 mH, R = 10.0 Ω.
    (b) Capacitive load: C= 300.0 uF, R = 10.0 Ω.
  - Non-linear Load: A 5.0 % reactor is used in the ac side a diode bridge rectifier with a capacitive filter, $C_{dc} = 940.0\ \mu$F, $R_{Load} = 22.0\ \Omega$.

Figures (3.16-3.17) show some relevant waveforms for the power conditioner when operating with the standard hysteresis current control with a linear inductive load. A hysteresis window of 5% of the rated peak reactive current component (i_{Lq}) has been used in each case.

One sees in figure 3.16 that the current of a linear load can be effectively decomposed in its active and reactive components by using the circuit depicted in figure 3.12. Further, the figure shows that the current injected in the ac mains by the power conditioner (i_f) follows closely the command current (i_c) and that yields almost total compensation of the reactive power drawn by the load, with an increase in the total power factor from 0.74 to 0.99 as shown in figure 3.17a. Moreover, the measured average switching frequency was 2.0 kHz, which agrees with the results obtained from the curves resulting from the design optimization.

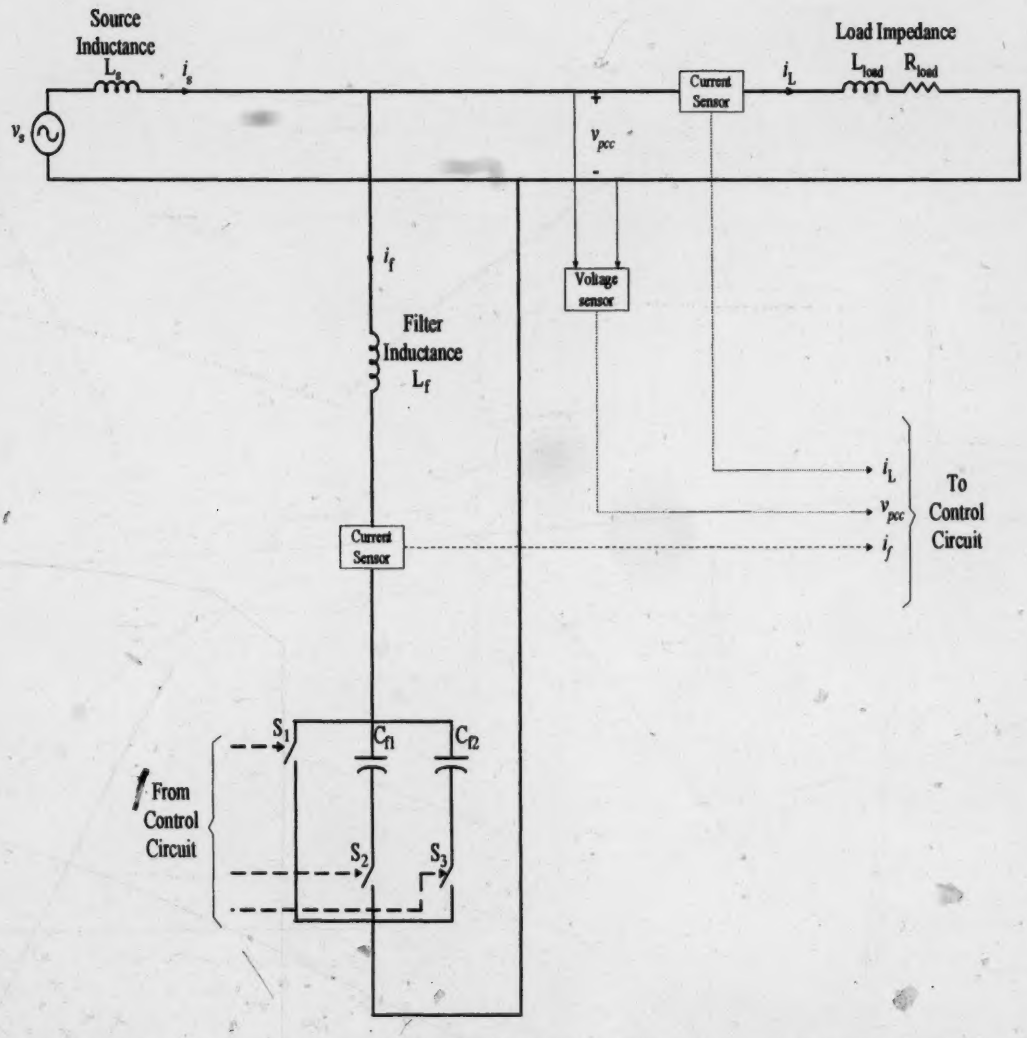


Figure 3.15 Main elements of the power circuit of SC power conditioner simulation system.

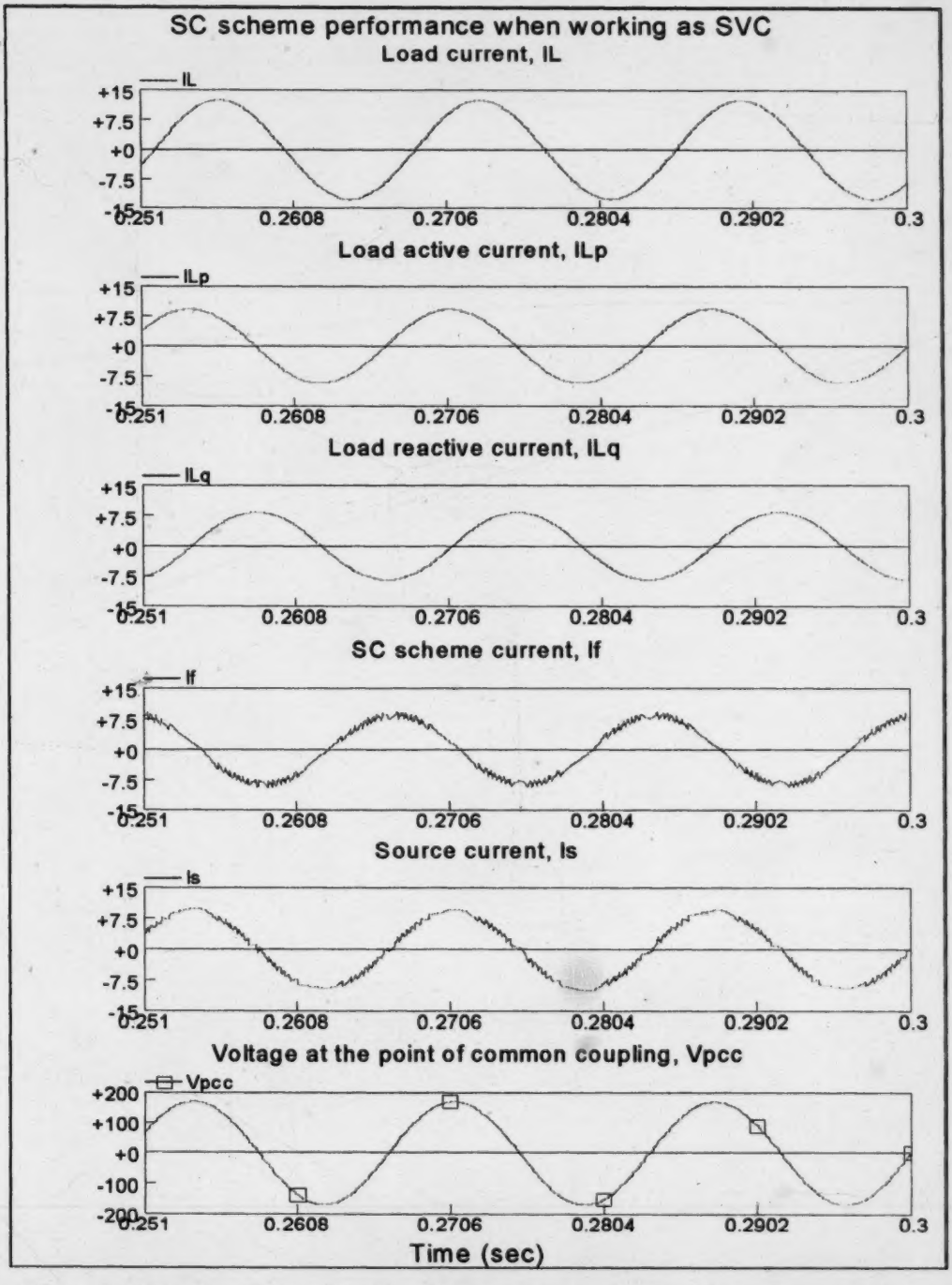
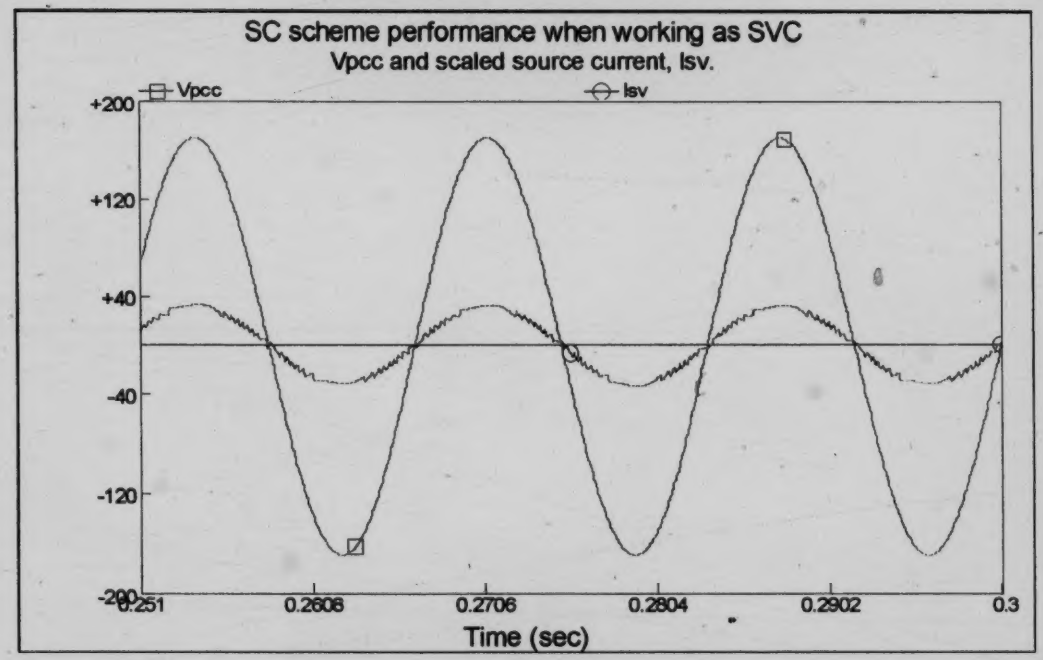
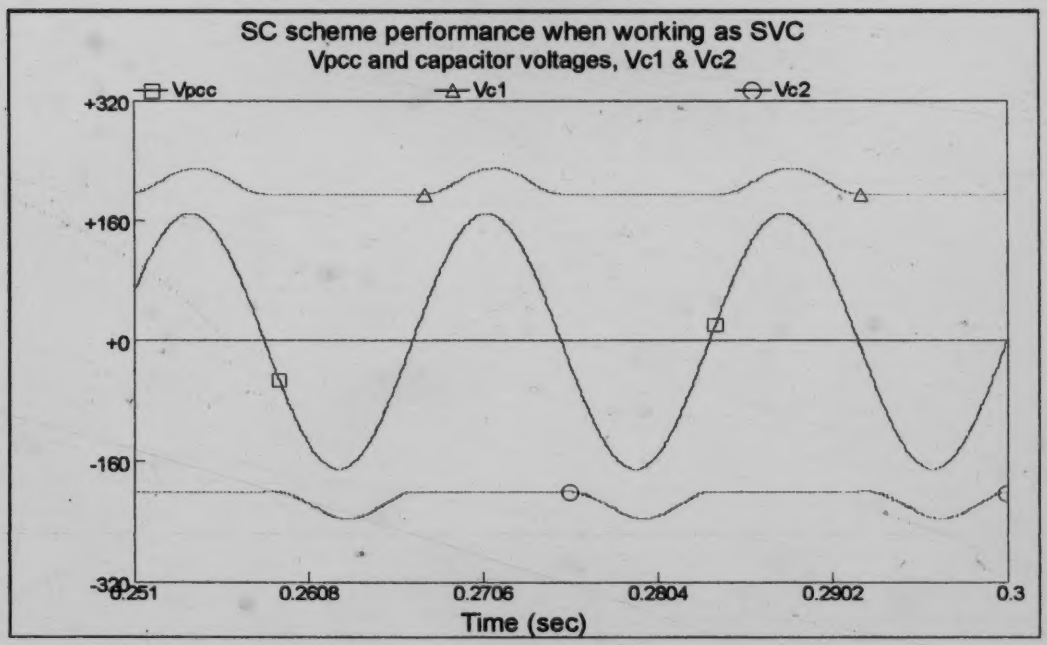


Figure 3.16 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c, and Voltage at the point of common coupling v_{pcc}, for a ***linear inductive load.***



(a)



(b)

Figure 3.17 SC performance with an ***inductive load***

(a) v_{pcc} and source current, i_s.

(b) v_{pcc} and capacitor voltages (v_{c1} & v_{c2})

However, it was found that the THD for i_s was measured as 3.8%. Finally, one sees in figures 3.17b that the peak values for the capacitor voltage waveforms are below the design specification (600 V).

Similar results can be shown in figure 3.18 and figure 3.19 when the SC power conditioner works with a capacitive load with 0.75 leading power factor. The SC scheme could achieve its function and improving the power factor to almost 0.99. It is worth mentioning that the SC is injecting a lagging current in this case that makes the capacitor voltages to decrease. Careful design for the passive elements should avoid the capacitor voltage to be less than the peak of the supply voltage.

Finally, figure 3.20 and figure 3.21 show the current and voltage waveforms at the same points in the circuit for the power conditioner operating as an active filter for a single-phase rectifier bridge with a capacitive filter. The reference current generating circuit is again able to separate the non-active from the active component of the load current as shown in figure 3.20. Moreover, the source current waveform presents a THD of 7.7%, for a load current with a THD of 58.0%. The THD could not be further attenuated due to the small voltage available to increase/decrease the filter current during zero voltage crossings of the PCC voltage and the small difference between the capacitor and supply voltages that adds more distortion at the peaks of the supply voltages.

The average switching frequency in this case is 3.3 kHz. Finally, one can also see that the capacitor voltage waveforms are quite similar to those seen in the SVC case as can be seen from figure 3.21b.

3.6 Limitations of the Proposed Scheme

Although the SC scheme could perform its function, reactive power compensation and harmonic mitigation, effectively, there are some drawbacks and observations found during the simulation:

- There is a drift in the initial capacitor voltage, V_{C0}, from the designed value, and this could be due to several factors. For example, the reference generation circuit provides some active current during the beginning of its operation, until reaching steady state, which affects this voltage.

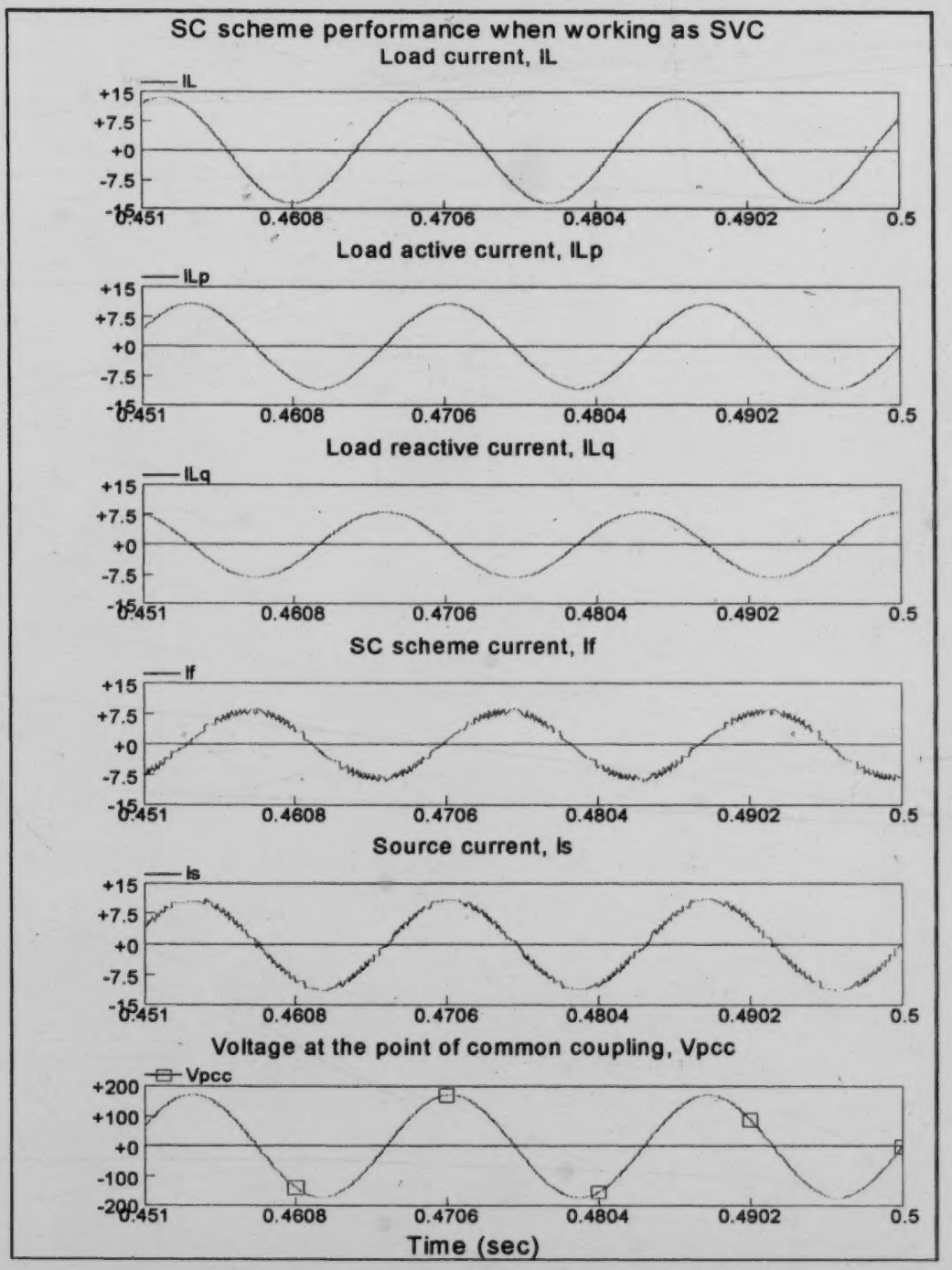
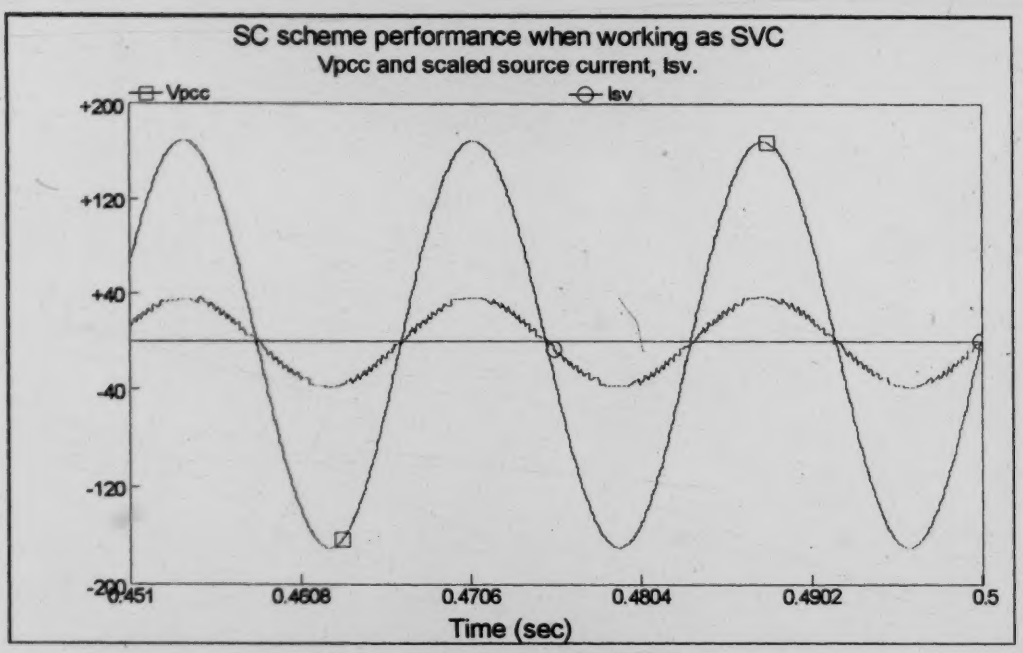
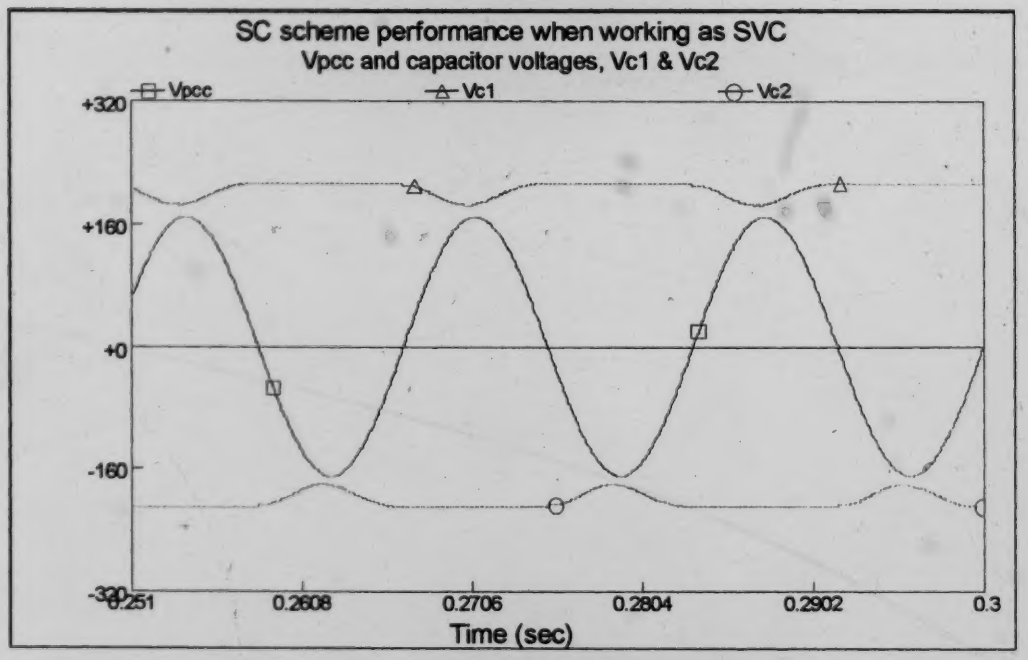


Figure 3.18 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c, and Voltage at the point of common coupling v_{pcc}, for a ***linear capacitive load.***



(a)



(b)

Figure 3.19 SC performance with a ***capacitive load***

(a) v_{pcc} and source current, i_s.

(b) v_{pcc} and capacitor voltages (v_{c1} & v_{c2})

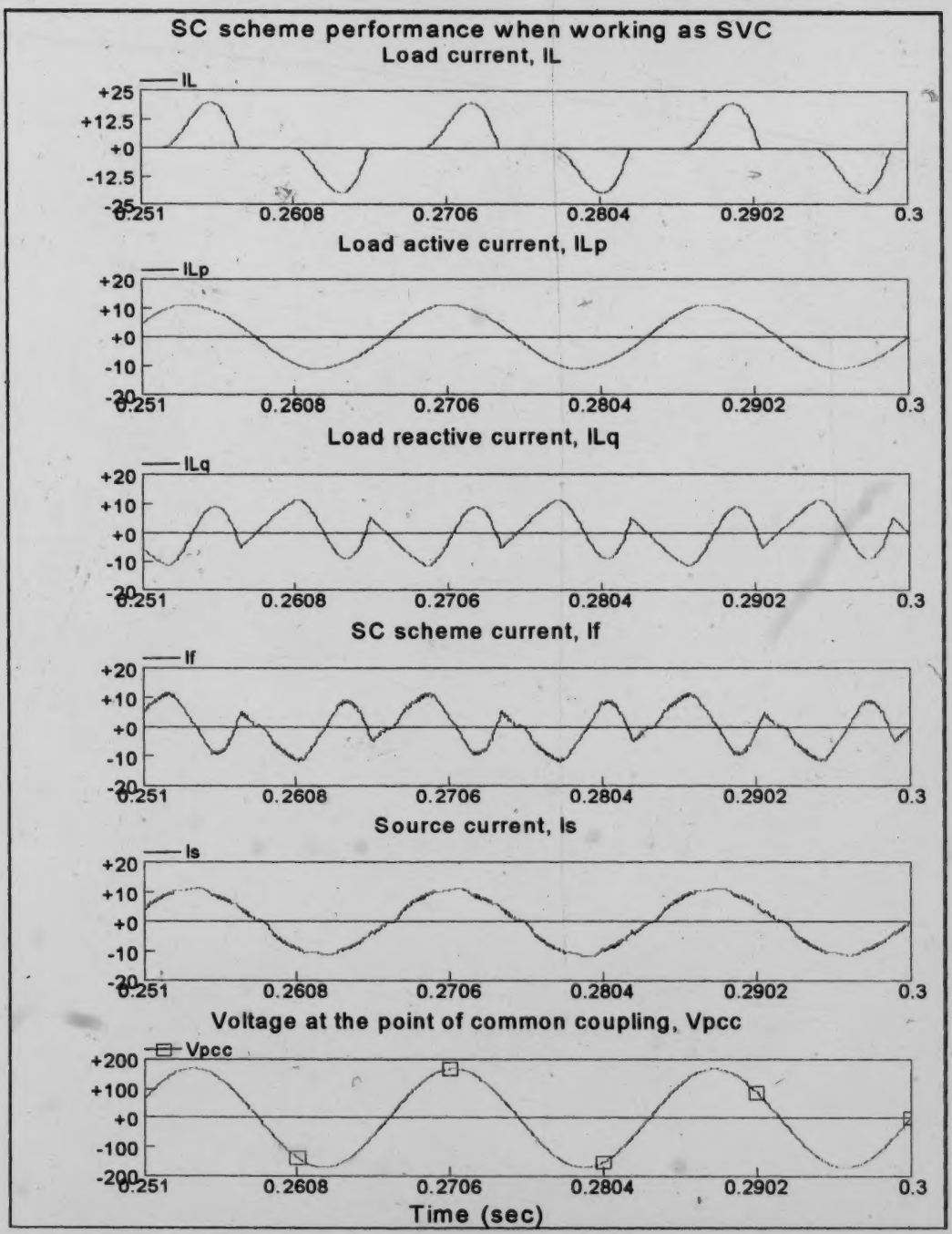
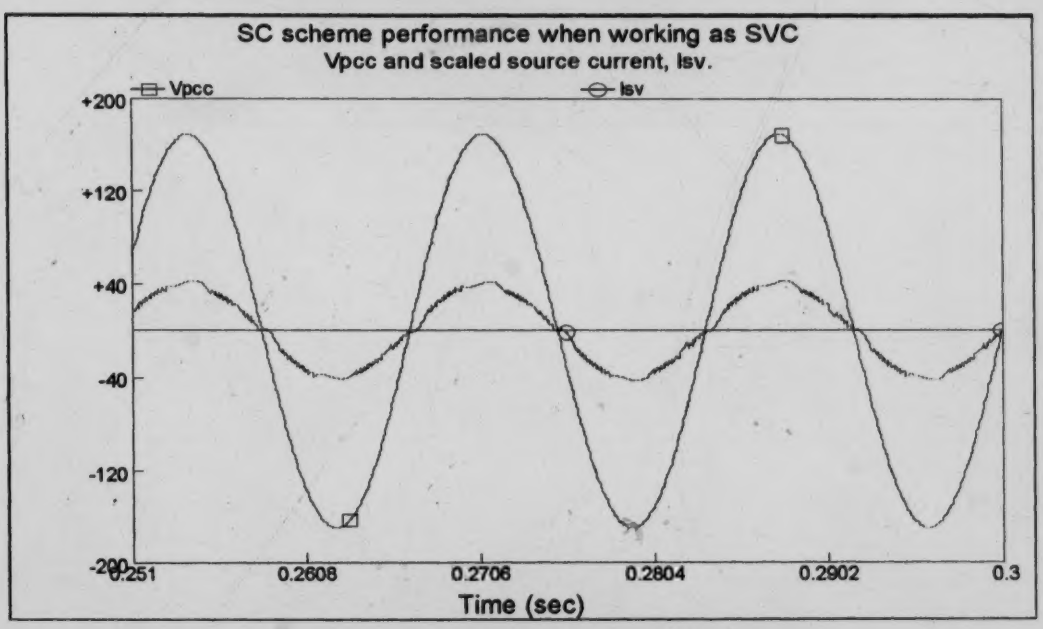
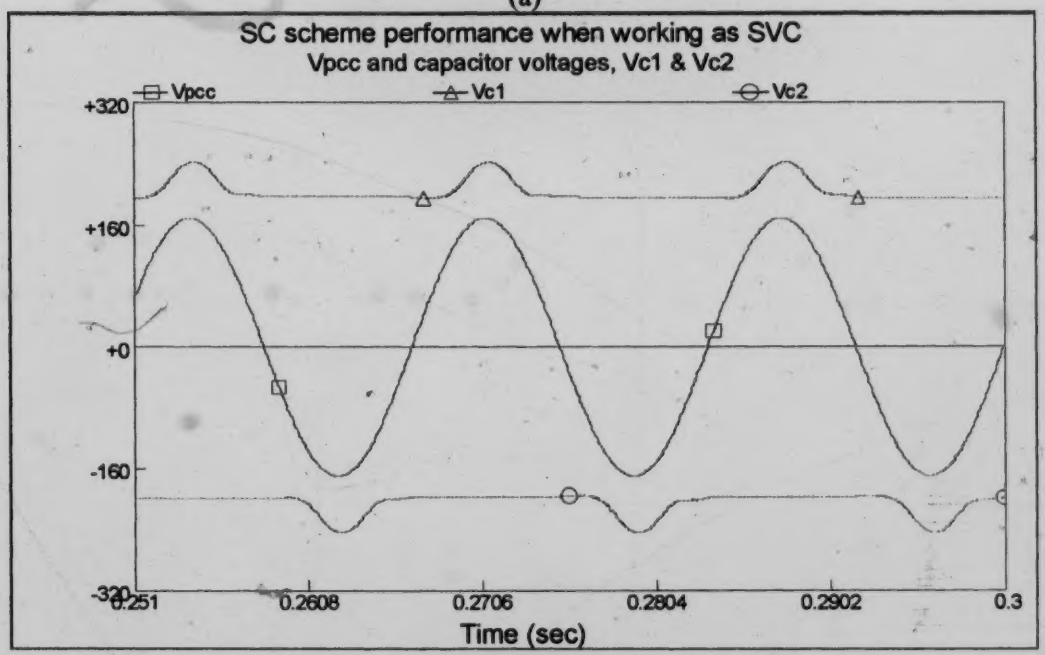


Figure 3.20 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c, and Voltage at the point of common coupling v_{pcc}, for ***a diode bridge rectifier with capacitor filter load.***



(a)



(b)

Figure 3.21 SC performance with ***a non-linear load***

(a) v_{pcc} and source current, i_s.

(b) v_{pcc} and capacitor voltages (v_{c1} & v_{c2})

- The switches were assumed to be ideal in the design code.
- The passive elements were assumed to be ideal. However, the real components will have parasitic resistances that may add more complication to the control of capacitor voltage.
- The situation may become worse in the case of compensation for a capacitive load as there is a dip in the capacitor voltage and the minimum capacitor voltage becomes closer to the peak of v_{pcc} as shown in figure 3.19b. This may limit the capability of the SC scheme in terms of the maximum current that can compensate.
- Finally, another important limitation of the standard control as discussed in [68] is the reduced di/dt around the zero voltage crossing points, when S_1 is on and the magnitude of v_{PCC} is small as shown in figure 3.20. This adds more distortion to the actual scheme current that is reflected on the THD of the source current. This is clearer for the case of harmonic compensation than reactive power compensation where high di/dt is required to cope for fast changing load.

3.7 Experimental Set up

An experimental prototype is built to investigate the real performance of the SC scheme and to confirm the accuracy of the simulation. The power circuit configuration, the control system hardware, and the experimental results of the experimental prototype are described in this section.

3.7.1 Power Circuit

The power circuit consists of the following units:

- A single-phase regulated power source of 120V. The source inductance is measured to be 0.1 mH.
- The load is varied to follow almost the same loads used in the simulation.
- Switched capacitor scheme that employs three 15A, 600V IGBT switches. A diode rectifier, as shown in figure 3.22, accompanies each IGBT to form a bi-directional switch.

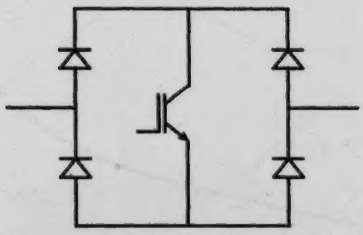


Figure 3.22 Bi-directional switch.

3.7.2 Voltage and Current Sensing

3.7.2.1 Voltage Sensing

Voltage sensing is normally done with voltage transformers. However, these transformers have the inherent disadvantage of phase shifting the waveform that may results in wrong detection of the zero crossing. Further, as the circuit is subjected to high frequency switching there exists some noise in the sensed voltage waveform that is called common mode voltage. Operational amplifier can be used to sense the voltage and this may solve the problem of phase shifting; however, a regular Op-Amp circuit doesn't reject the common mode voltage.

Therefore, the circuit shown in figure 3.23, which is recommended by [94], is used and it has both the advantage of no phase shifting and high capability of common mode voltage rejection.

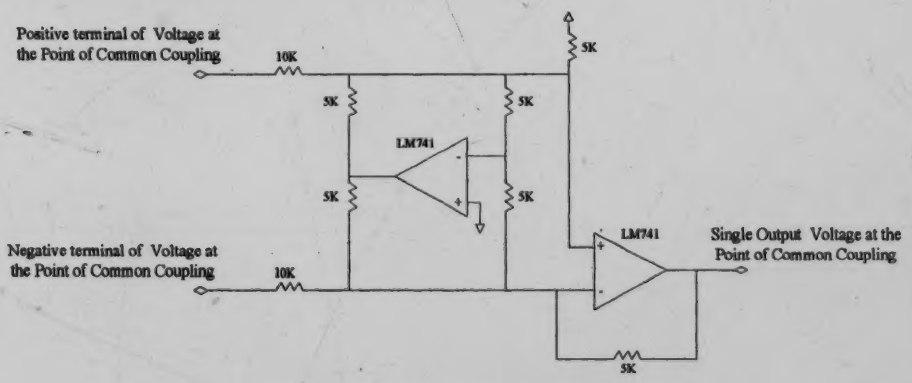


Figure 3.23 Supply voltage sensing circuit

3.7.2.2 Currents Sensing

The current sensing is done with high frequency current transducer called LEM LA 50-S, shown in figure 3.24, that is suitable for switching frequencies up to 100 kHz which ensure that correct measurement of the current flowing in the circuit.

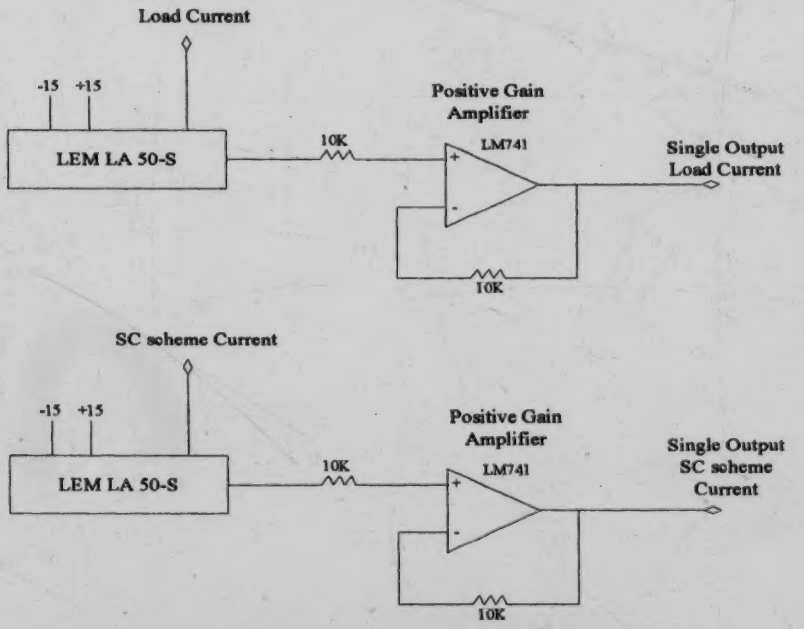


Figure 3.24 Load and filter currents sensing circuits.

3.7.3 Control Circuit

Figure 3.25 shows the schematic diagram of the control circuit hardware. It consists of four main sub circuits:

- ***Hysteresis comparator sub circuit***: this circuit compares between the command current and actual filter current to get the switching signal, OUT_1, which controls the three switches S_1, S_2, and S_3.
- ***Voltage zero crossing detector sub circuit***: this circuit is used to provide the control circuit with the moment, OUT_2 shown in the figure, to

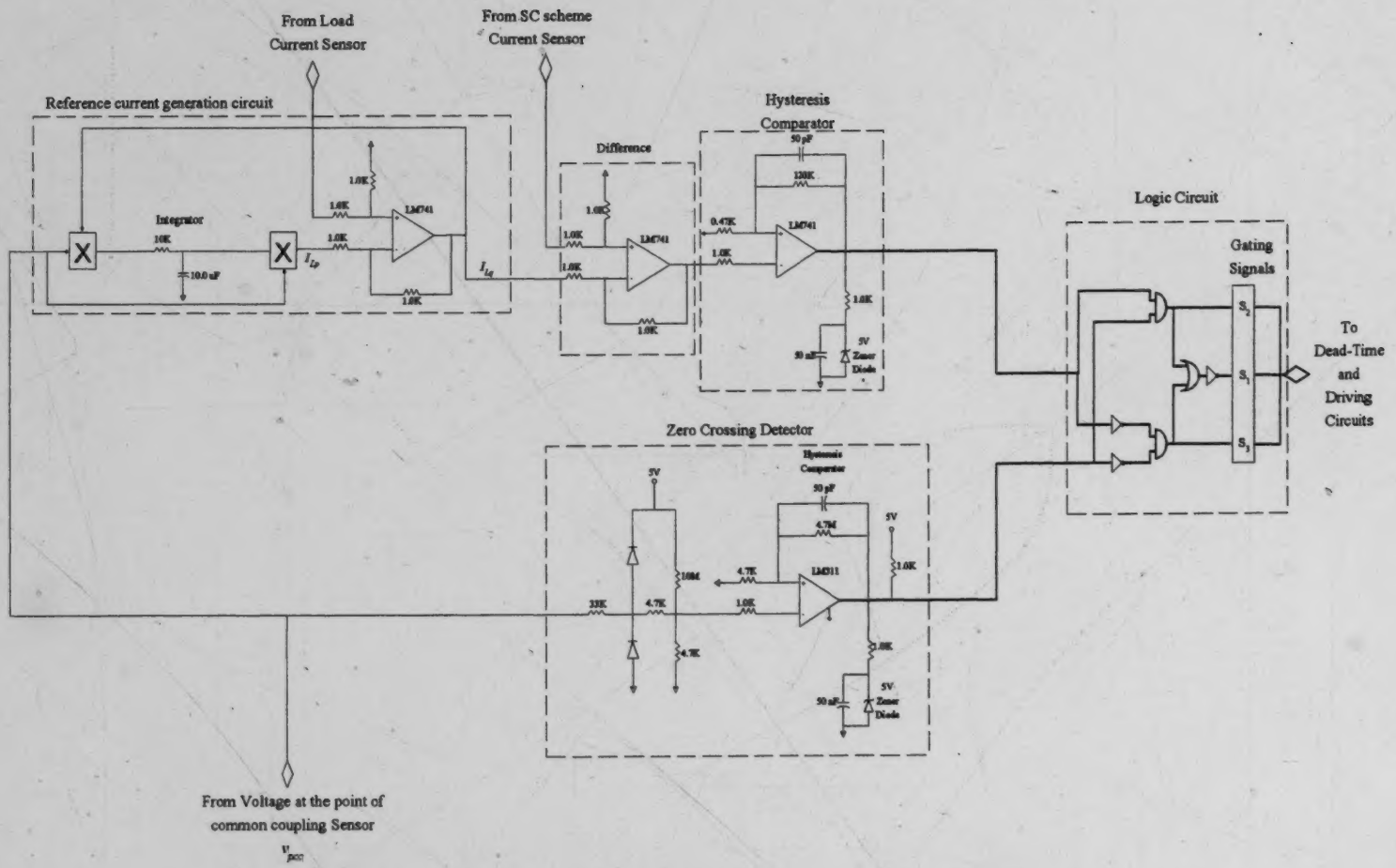


Figure 3.25 Control circuit hardware for reactive power compensation.

change control from positive cycle to negative cycle. It is designed according to [94].

- ***Reference generation circuit:*** that is designed according to section 3.4.1.
- ***Logic circuit***: the two outputs, OUT_1 and OUT_2, are provided to the logic circuit of the standard control strategy. The outputs from the logic circuits are the signals to three switches S_1, S_2, and S_3.

3.7.4 Dead-Time and Driving Circuits

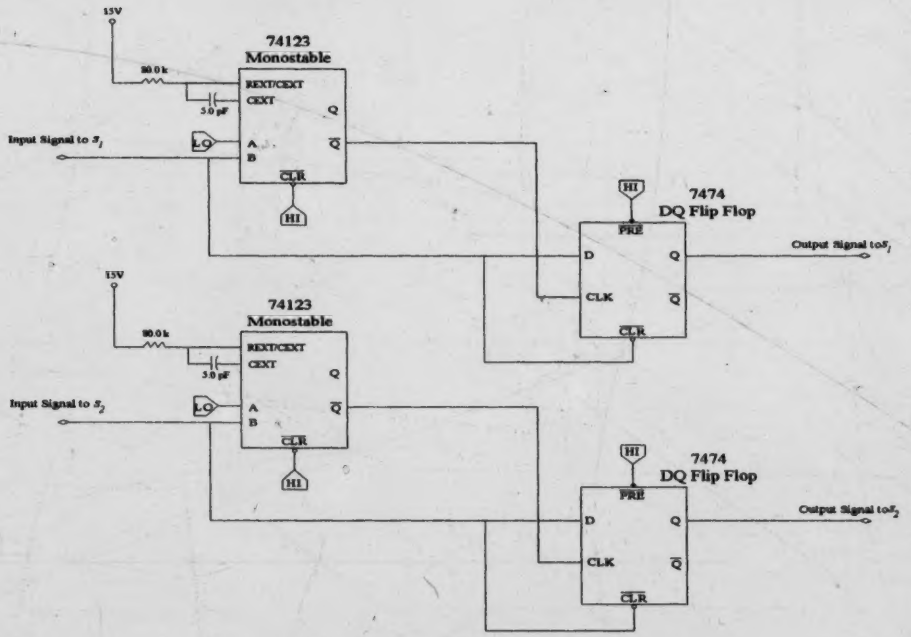
The power switches should operate with a dead-time and equipped with snubber circuits to ensure an alternative path for the inductor current during the commutations and to reduce the switching stress across the switches. The circuit that can provide the dead-time between the switches is shown in figure 3.26.

Finally, the output signals from the control circuit are at TTL level, which should be amplified to be able to meet the requirement of driving the IGBTs on and off. Further, the control circuit should be isolated from the power circuit to protect it from any failure in the power system. Therefore, separate isolated power supply should be used for the each IGBT and the signals to the three driver circuits should be isolated which can be done by using opto-isolators. The 6N135 opto-isolator, which incorporates high-speed logic circuits and has a propagation delay of 50 ns are suitable for this application. The complete drive circuit is shown in figure 3.27. It is worth mentioning that a 3.3V zener diode is used at the output of driver to ensure a negative voltage pulse to close the switch.

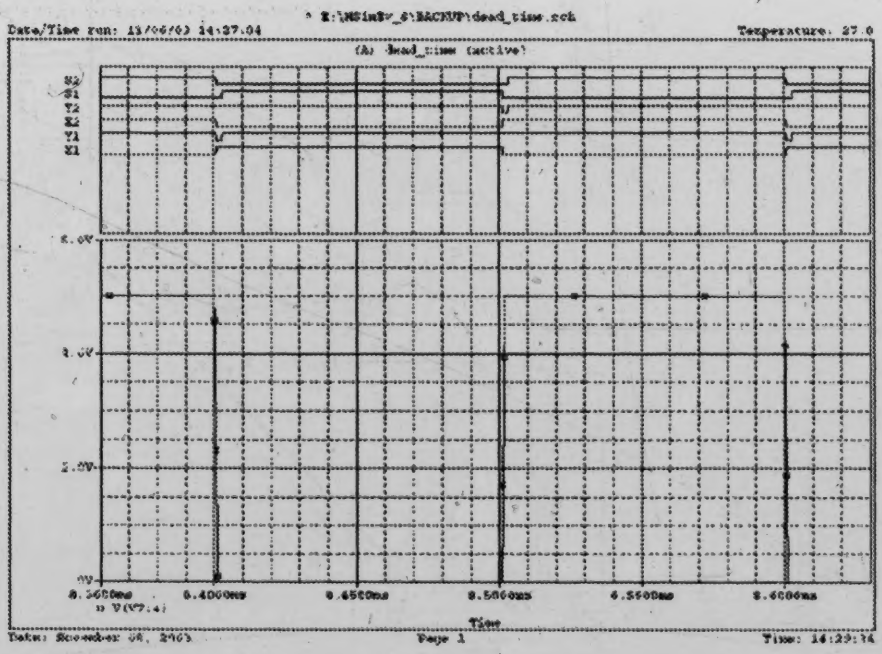
3.7.5 Experimental Results

3.7.5.1 Reactive Power Control

The waveforms in figure 3.28a,b illustrates the operation of the SC scheme for reactive power compensation of an inductive and a capacitive load respectively. The specification of the SC compensator, source and load are as follows:



(a)



(b)

Figure 3.26 (a) Experimental circuit that provide dead time between switches.

(b) PSPICE simulation results for the dead-time circuit.

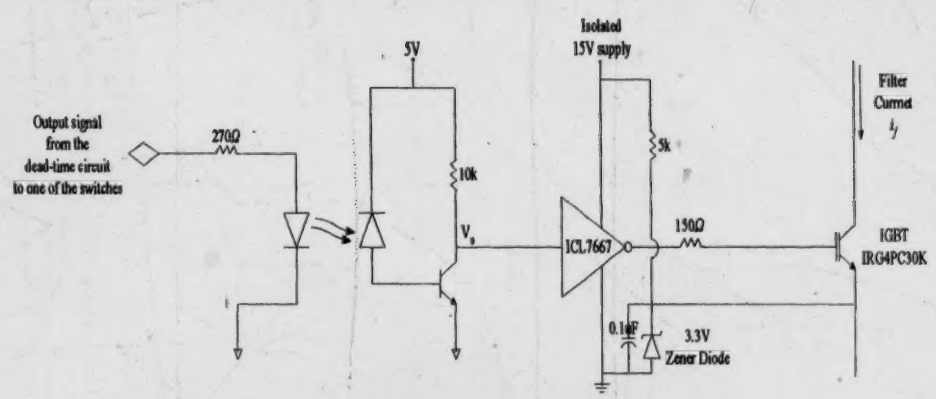


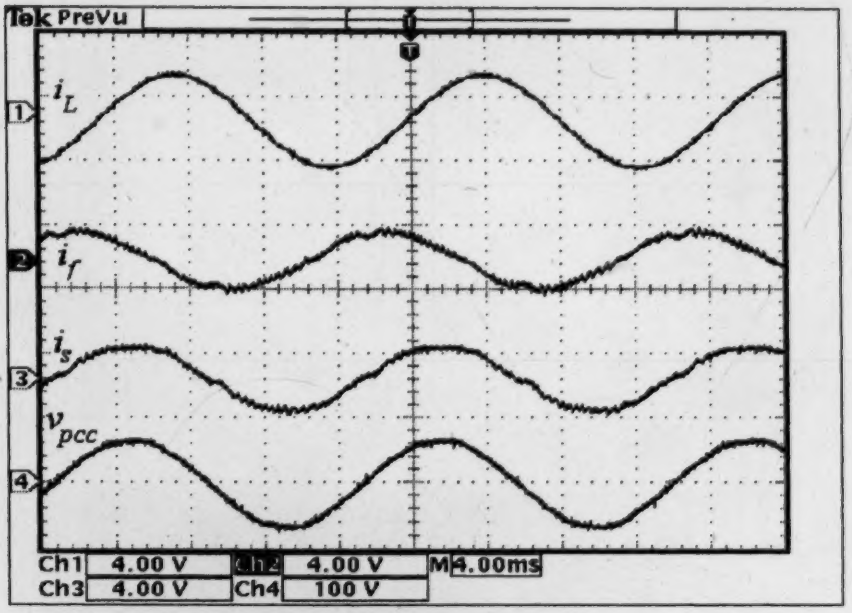
Figure 3.27 Driving circuit for an IGBT

- Utility system: A single-phase regulated power source of 120V, 60 Hz; Line resistance, R_s=0.1 Ω, Line inductance, L_s=0.1 mH.
- SC VAR compensator: L_f = 3.0 mH, C_f = 260.0 μF
- Load: Inductive load, L= 24 mH, R = 10.0 Ω , Capacitive load, C= 340.0 μF, R = 10.0 Ω.

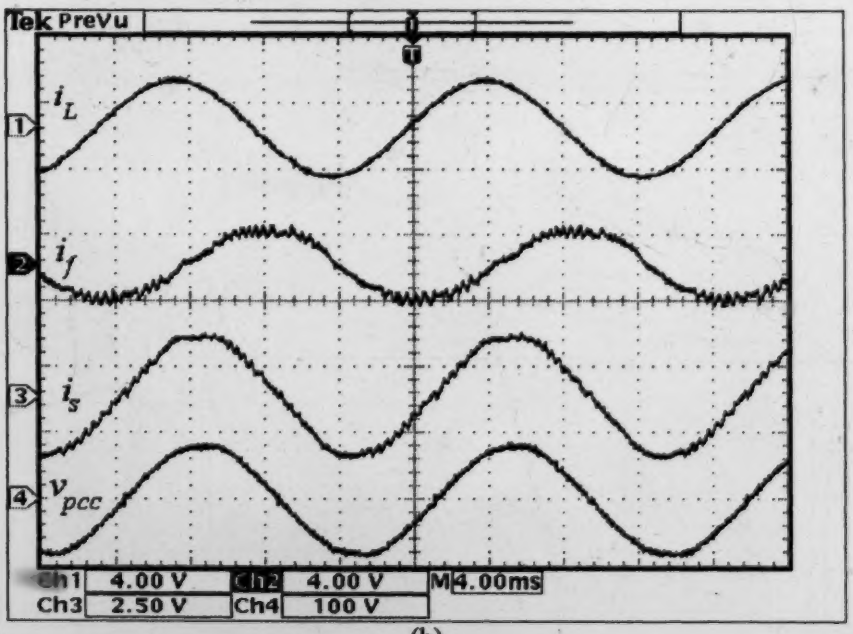
The load current (i_L), power conditioner current (i_f), supply current (i_s), and the voltage at the point of common coupling (v_{pcc}) are shown in these figures. It can be seen from the waveforms that the power conditioner generates currents that are 90° leading, figure 3.28a, or 90° lagging, figure 3.28b, with respect to its supply voltage, as predicted. Their magnitudes are such that the source current is almost in phase with the source voltage yielding an almost unity total power factor at the PCC. In fact the power factor improved from 0.74 lagging to 0.99 in the first case and from 0.78 leading to 0.99 in the second case.

However, the supply current presents mostly high frequency harmonics and a THD of 5.4% and 4.4% for both cases respectively. This happens due to the poor tracking ability of the scheme during the period of small vpcc and the lower capacitor voltage that reduce the tracking capability during the peaks of the vpcc.

It is worth mentioning that the proposed power conditioner achieved reactive power compensation with low harmonic distortion despite an average switching frequency of only 1.9 kHz as shown in figure 3.29. An even lower



(a)



(b)

Figure 3.28 Load current, power conditioner current, supply current and supply voltage respectively with (a) inductive load (L = 24 mH, R = 10 Ω), (b) capacitive load (C = 340 uF, R = 10 Ω).

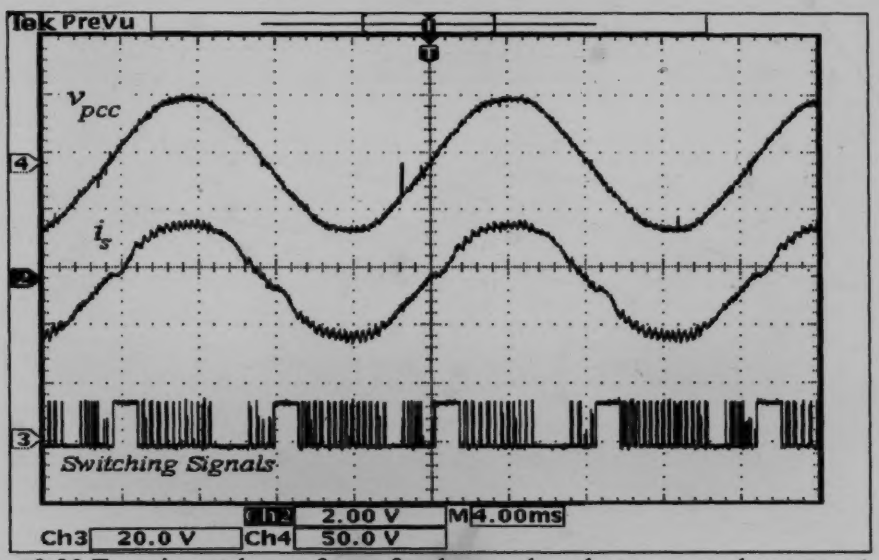


Figure 3.29 Experimental waveforms for the supply voltage $v_{s,}$ supply current i_s, and switching signals.

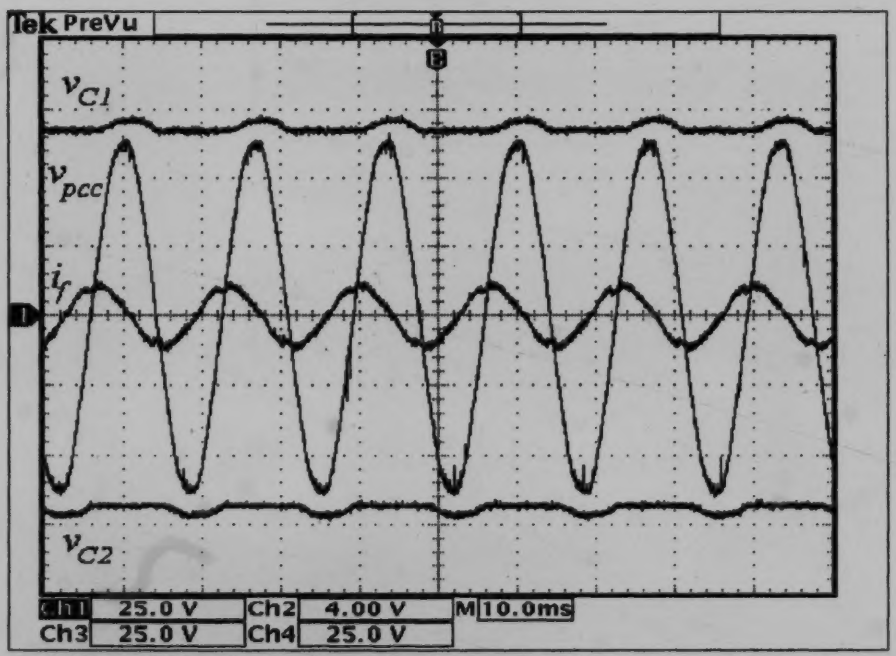


Figure 3.30 Experimental waveforms for the supply voltage v_s, capacitor voltages, v_{c1} & v_{c2}, and power conditioner current i_f for a capacitive reference current.

THD can be obtained by decreasing the hysteresis window at the expense of higher switching losses.

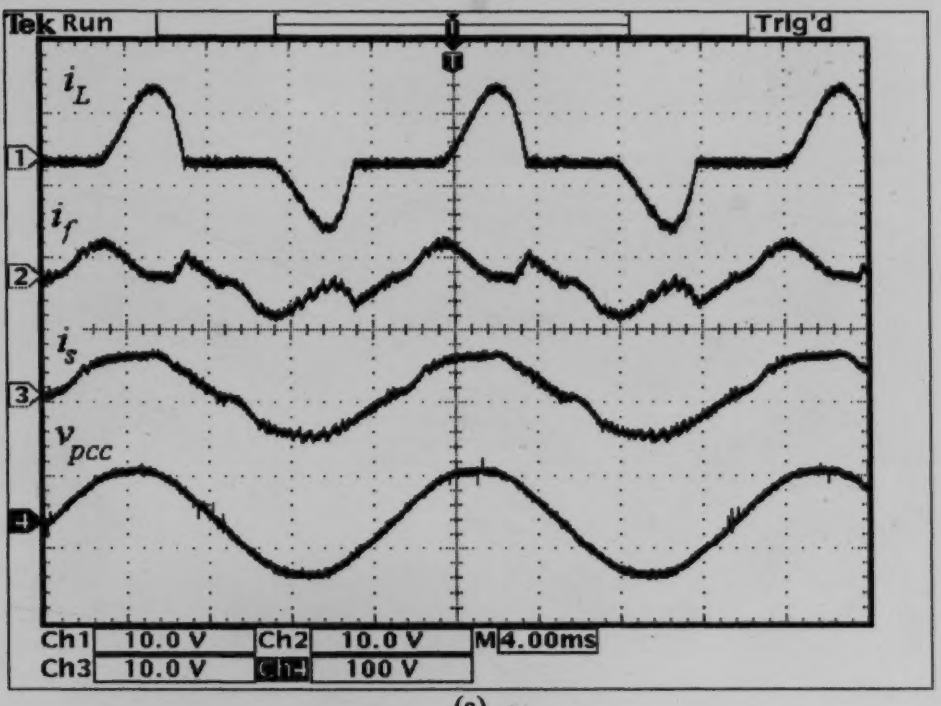
The capacitor voltage waveforms, v_{c1} and v_{c2}, along with the v_{pcc} and power conditioner current are shown in figure 3.30 for the inductive load case, which shows that the SC control circuit could keep the capacitor voltages always higher than the peak of v_{pcc} to perform its function properly.

3.7.5.2 Harmonic Mitigation and Reactive Power Control

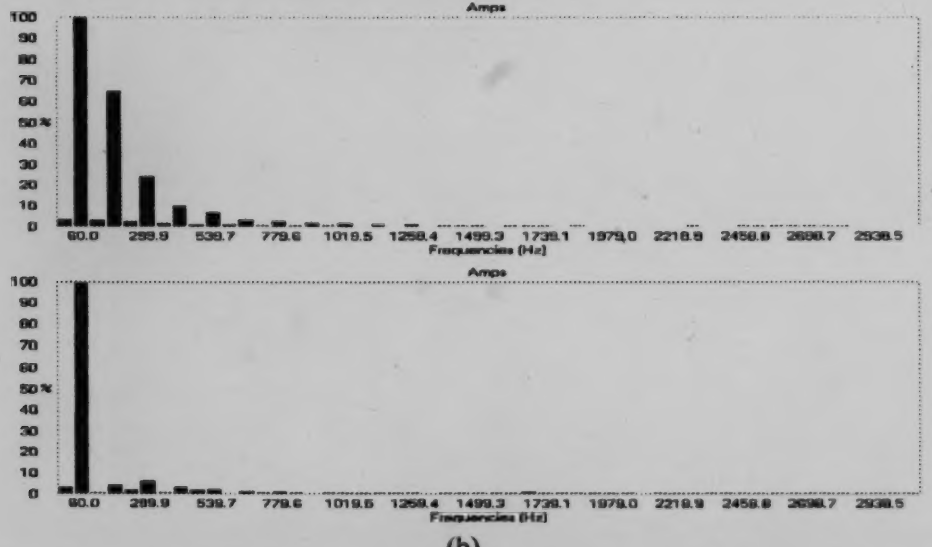
The proposed power conditioner was also evaluated for compensating common non-linear loads such as single-phase diode rectifiers with a capacitive dc filters. The rectifiers usually present a series reactor in the ac side to reduce the injected current harmonics that result in a lagging displacement power factor. Figure 3.31 show that the proposed power conditioner can compensate for the current harmonics and reactive power at the same time.

A 5.0 % reactor is used in the ac side of a diode bridge rectifier with a capacitor filter, $C_{dc} = 940.0\ \mu F$, $R_{Load} = 22.0\ \Omega$.

Figure 3.31a shows the waveforms of the load current, power conditioner current, source current, and supply voltage for a single-phase rectifier bridge with a capacitive filter. The THD of the input current of the rectifier (i_L) is 57.8%. The power conditioner reduces the THD of the source current to 7.8%, and improves the total PF to 0.98. As can be seen in the spectrum of figure 3.31b, the main source current harmonic is of third order, which has already been reduced by 95%. Further attenuation is difficult to achieve mostly due to the small voltage available to increase/decrease the filter current during zero voltage crossings of the PCC voltage.



(a)



(b)

Figure 3.31 (a) Load current, power conditioner current, supply current and supply voltage with rectifier bridge with capacitive filter load with standard control strategy, (b) Harmonic spectrum for both load and supply current.

3.8 Conclusions

A new single-phase topology that is based on switched capacitor technology and can be used for reactive power compensation and harmonic mitigation is presented. It presents a simple power structure, only three bi-directional switches and two small capacitors, and can be controlled with standard hysteresis current control.

Although the power structure and control strategy are very simple, the modeling of the system is rather complicated due to the L-C interaction and the different possible currents that can be used as templates for hysteresis control. This prompted the use of a design approach based on a detailed code for simulating currents and voltages in the circuit and a systematic optimization procedure that can allow the choice of the system components for different applications.

Nevertheless, the new control strategy presents some drawbacks that limit the operation of the SC scheme. The current poor tracking capability of the scheme at the worst possible case for switched capacitor topologies: the zero crossing points of the ac line voltage, and the uncontrolled capacitor voltages are the major disadvantages of the proposed circuit that were observed during the simulation process.

Although these limitations have a negative effect of adding some distortion to the source current waveform, the SC scheme could provide dynamic inductive, capacitive and harmonic currents to compensate for reactive currents and harmonics distortion.

Finally, the experimental results confirm the observation concluded from the simulation and shows the performance of the SC scheme for different loading conditions.

CHAPTER 4

The Proposed Scheme and Modified Control Strategy

4.1 Introduction

This chapter presents a modified switching scheme that aims to mitigate some of limitations presented by the standard hysteresis control presented in Chapter 3. The new control circuit aims to:

- increase the capability of SC scheme for following command signals with high derivatives around the zero-crossing points of the voltage at the point of common coupling, especially for non-linear loads.
- control the capacitor voltages to maintain it at certain level above the peak of the supply voltage to improve the SC scheme controllability.

Steady-state operation and transient analysis are carried out to analyze the performance of the scheme under different operating conditions. Finally, experimental results are provided to demonstrate the validity of the analysis and design procedure.

4.2 Modified Control Strategy

4.2.1 Modified Logic Circuit

One limitation of the control strategy proposed in Chapter 3, as discussed in [68], is the reduced di/dt around the zero voltage crossing points, when S_1 is on and the magnitude of v_{PCC} is small. Using the logic shown in figure 4.1, where S_2 and S_3 are switched complementarily for a small period around the zero voltage crossings, can reduce this problem. Higher values of di/dt are achieved due to the high voltages present across the capacitors. For the rest of the half cycle the switching follows the same principle as in figure 3.10.

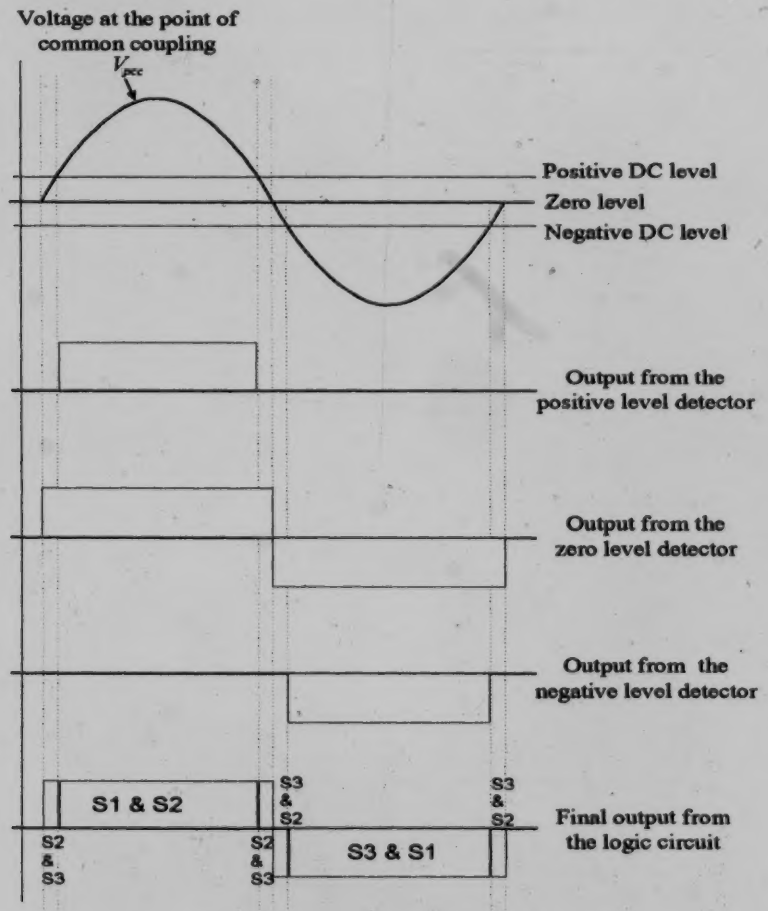


Figure 4.1 Modified switching strategy for the power conditioner.

Therefore, the SC scheme will have four modes of operations, as shown in figure 4.2, as follows:

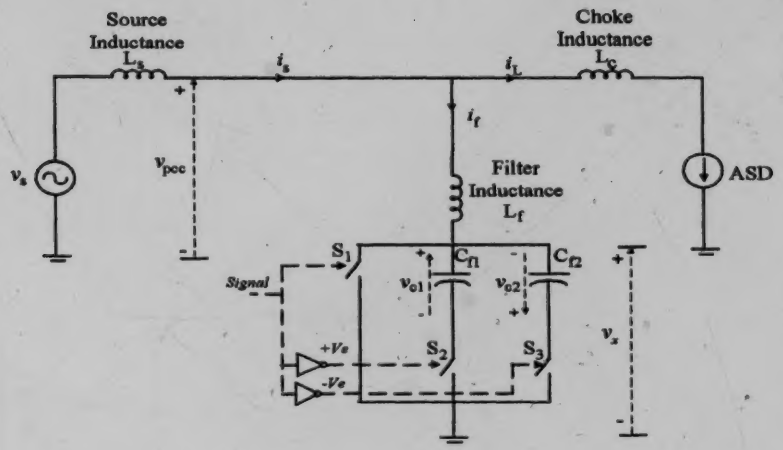
For the positive cycle of the of voltage at the point of common coupling,

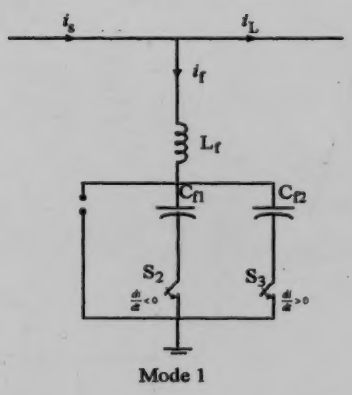
- **Mode 1: when $0<v_{pcc}<+V_{dc}$:**
  - S_1 is off. When S_3 is on, S_2 is off, $v_{coil} = v_{pcc} + V_{c2}$ and the rate of rise of current, di/dt>0.
  - S_1 is off. When S_3 is off, S_2 is on, $v_{coil} = v_{pcc} - V_{c1}$ and the rate of rise of current, di/dt<0.
- **Mode 2: $v_{pcc}>+V_{dc}$:**
  - S_3 is off. When S_1 is on, S_2 is off, $v_{coil} = v_{pcc}$ and the rate of rise of current has the same polarity of v_{pcc}, di/dt>0.
  - S_3 is off. When S_1 is off, S_2 is on, the rate of rise of current has the opposite polarity of v_{pcc} since, $v_c > |v_{pcc}|$, di/dt<0.

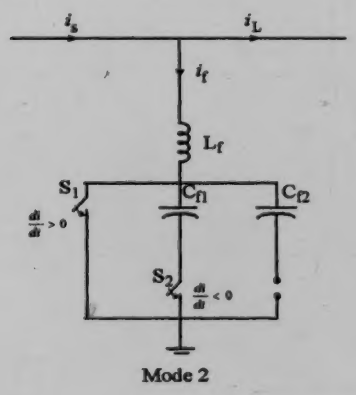
For the negative cycle of the of voltage at the point of common coupling:

- **Mode 3: when $-V_{dc}<v_{pcc}<0$:**
  - S_1 is off. When S_2 is on, S_3 is off, $v_{coil} = v_{pcc} - V_{c1}$ and the rate of rise of current, di/dt<0.
  - S_1 is off. When S_2 is off, S_3 is on, $v_{coil} = v_{pcc} + V_{c2}$ and the rate of rise of current, di/dt>0.
- **Mode 4: $v_{pcc}<-V_{dc}$:**
  - S_2 is off. When S_1 is on, S_3 is off, $v_{coil} = v_{pcc}$ and the rate of rise of current has the same polarity of v_{pcc}, di/dt<0.
  - S_2 is off. When S_1 is off, S_3 is on, the rate of rise of current has the opposite polarity of v_{pcc} since, $v_{c2} > |v_{pcc}|$, di/dt>0.

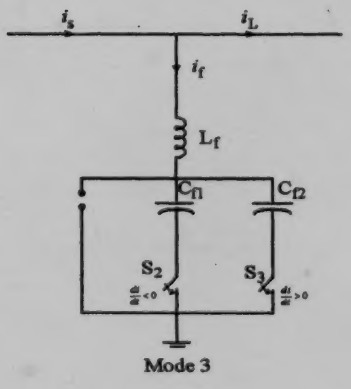
Finally, the circuit that implements this modified switching strategy is shown in figure 4.3. For the positive semi cycle, the output of the positive level and zero level detectors are fed once to an XOR gate to get the small periods after and before the zero crossings of the voltage at the point of common coupling, and are simultaneously fed to an AND gate to get the switching during the rest of the semi cycle. The same logic applies to the negative semi cycle.

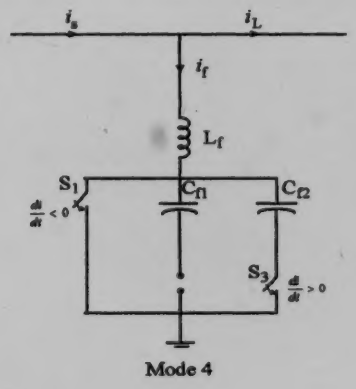






$$v_{pcc} > 0$$





$$v_{pcc} < 0$$

Figure 4.2 Modes of operation for the modified control strategy.

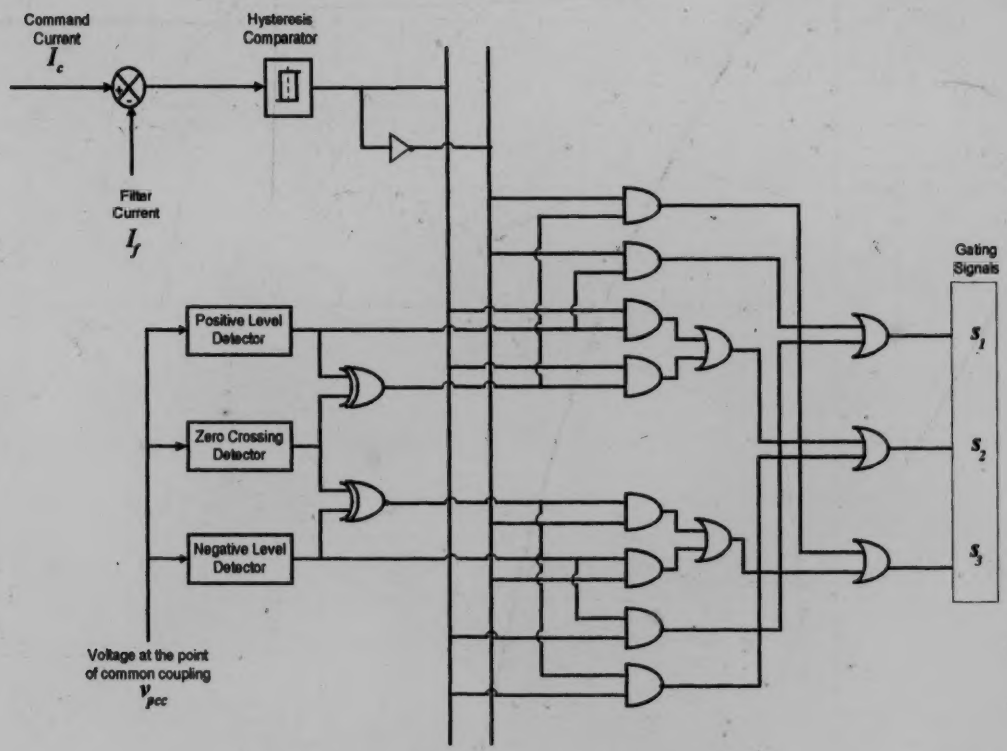


Figure 4.3 Modified Logic circuit implementation.

4.2.2 Capacitor Voltages Regulation

For controlling the capacitor voltages, the scheme has to be provided with some active current (regulating current) to maintain the voltage at the required level [22]. The regulation current i_{reg}(t) for the SC scheme is provided by the modified control strategy as shown in figure 4.4. Assuming the converter to be loss-free, as ideally it provides only the reactive power to the load, and that the hysteresis window is very small, one can say, that the capacitor voltage will be charged up to a certain voltage level that depends on the initial start up process and keep this charge for the rest of the operation. However, because the reference generation circuit provides some active current during the beginning of its operation, until reaching steady state, and converter has switching loss, the capacitor voltage drifts from this level.

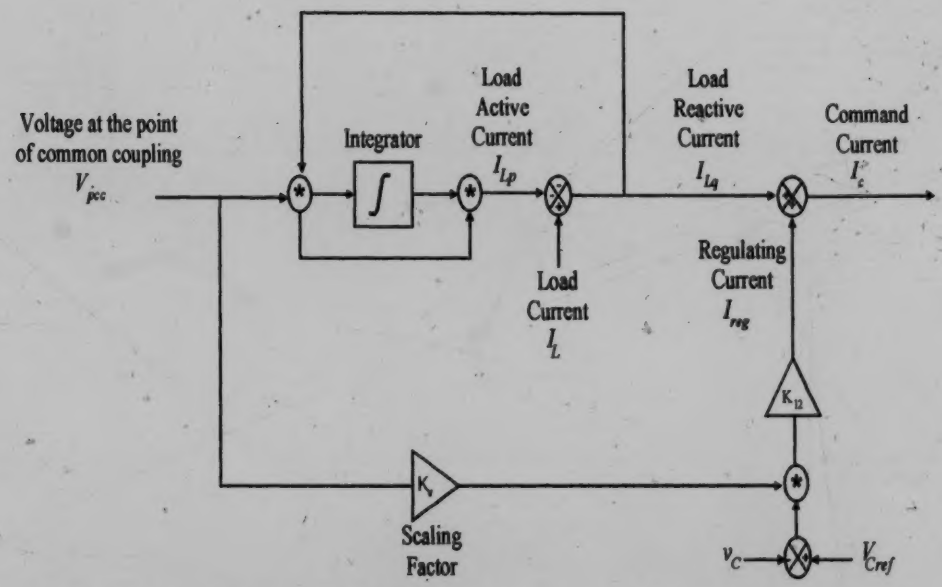


Figure 4.4 Capacitor voltage regulation by the modified control strategy.

Therefore, the utility must supply not only the real power of the load current, but also a small overhead for the capacitor leakage and converter switching losses. This way, the initial capacitor voltage can be maintained at a certain required level that meets the design criteria and allow the SC scheme to work properly under different operating conditions. Using the energy balance principle, the control strategy for regulating the capacitor voltages can be described as follows:

If the reference voltage to the capacitor is V_{cref}, then the reference energy storage will be

$$E_{cref}(t) = \frac{1}{2} C V_{cref}^2 \tag{4.1}$$

While the instantaneous energy in the capacitor is

$$E_c(t) = \frac{1}{2} C v_c^2 \tag{4.2}$$

Therefore, the energy loss of the capacitor in one period will be

$$\begin{aligned}\Delta E_c(t) &= E_{cref} - E_c(t) \\ &= \frac{C}{2}\left(V_{cref}^2 - v_c^2(t)\right) \\ &= \frac{C}{2}\left[\left(V_{cref} + v_c(t)\right)\left(V_{cref} - v_c(t)\right)\right]\end{aligned} \tag{4.3}$$

Assuming that, within one period, the variation in capacitor voltage is moderate, the term [V_{cref} + v_c(t)] can be approximated as:

$$\begin{aligned}V_{cref} + v_c(t) &\approx 2V_{cref} \\ \Delta E_c(t) &\approx CV_{cref}\left(V_{cref} - v_c(t)\right) \\ &= K_1\left(V_{cref} - v_c(t)\right)\end{aligned} \tag{4.4}$$

Since this energy loss must be supplied by the utility voltage source, the peak value of the charging current I_{reg} can be estimated as follows:

$$\int_0^T V_s \sin \omega t I_{reg} \sin \omega t dt = \Delta E_c \tag{4.5}$$

Therefore

$$I_{reg} = \frac{2}{TV_s}\Delta E_c = K_2 \Delta E_c \tag{4.7}$$

where

$$K_2 = \frac{2}{TV_s}$$

Hence, the peak value of the charging current I_{reg} can be obtained as in the following

$$\begin{aligned}I_{reg} &= K_2 \Delta E_c = K_2 K_1\left(V_{cref} - v_c(t)\right) \\ &= K_{12}\left(V_{cref} - v_c(t)\right)\end{aligned} \tag{4.8}$$

where

$$K_{12} = \frac{2CV_{cref}}{TV_s}$$

Finally, the regulating current (I_{reg} $\sin\omega t$) is added to the reference current to get the final current command to the filter. The complete circuit implementation of the modified control strategy is shown in figure 4.5.

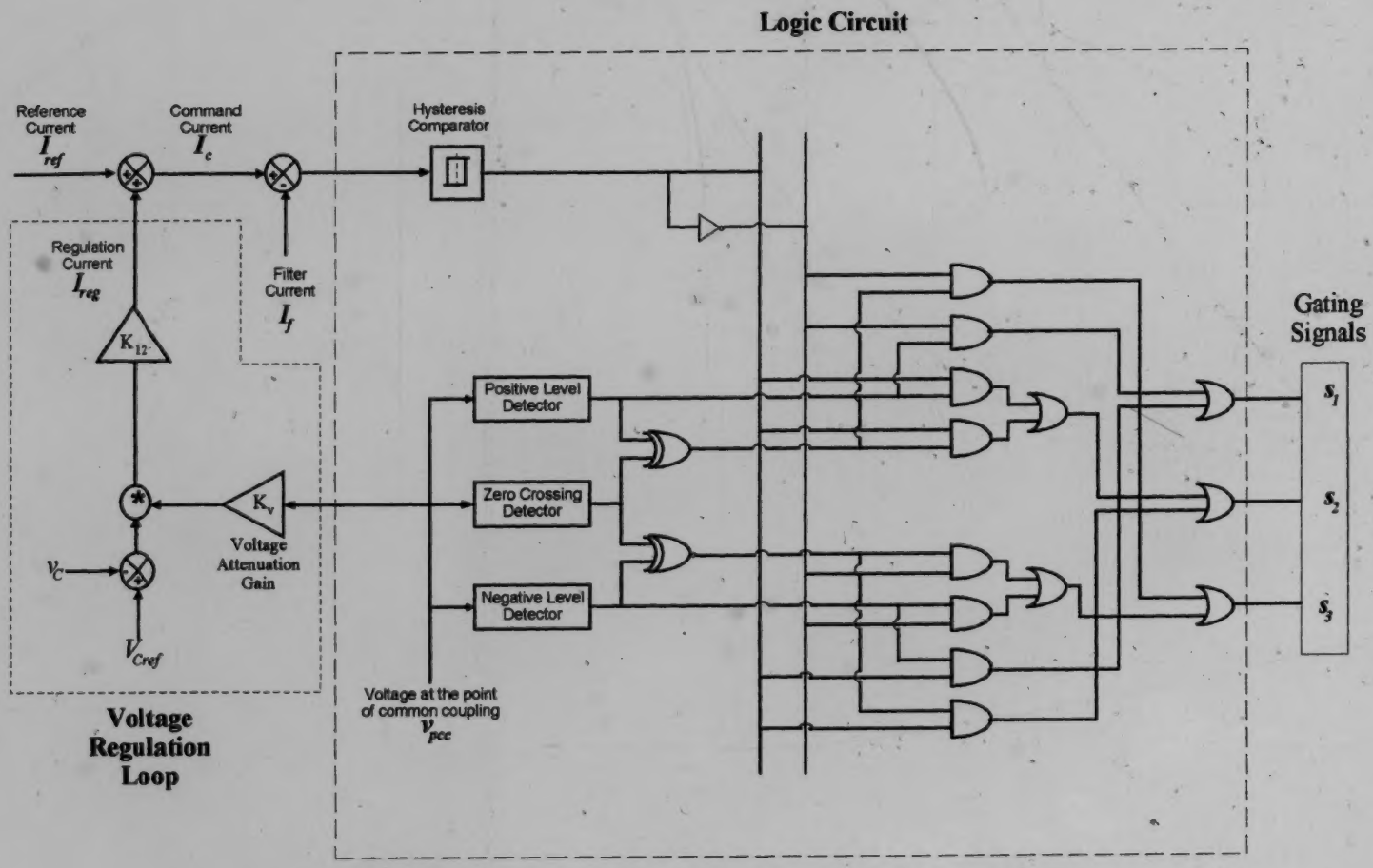


Figure 4.5 The complete circuit implementation of the modified control strategy.

4.3 Designing the SC Scheme with the Modified Control Strategy

4.3.1 Deriving Design Equations for the Modified Control Strategy

The current and voltage equations will be driven for the two modes of operation of the SC scheme in the positive half cycle as they are the same for the negative cycle but with negative logic. The equations can be driven as follows:

- **Mode 1:** ($0<v_{pcc}<+V_{dc}$)
  - ***When di/dt>0***

$$i_{f_K}(t) = G_{II}\sin(\omega t - \gamma_{II}) + e^{-\alpha^{II}t}\left(A_{1k}\cos|\beta|t + A_{2k}\sin|\beta|t\right) \quad (4.9)$$

$$v_{C2_K}(t_k) = \frac{1}{C_f}\int_{t_{k-1}}^{t_k} i_{f_K}(t_k)\,dt + V_{C20_{k-1}} \quad (4.10)$$

  - ***When di/dt<0***

$$i_{f_K}(t) = G_{II}\sin(\omega t - \gamma_{II}) + e^{-\alpha^{II}t}\left(A_{1k}\cos|\beta|t + A_{2k}\sin|\beta|t\right) \quad (4.11)$$

$$v_{C1_K}(t_k) = \frac{1}{C_f}\int_{t_{k-1}}^{t_k} i_{f_K}(t_k)\,dt + V_{C10_{k-1}} \quad (4.12)$$

- **Mode 2:** ($v_{pcc}>+V_{dc}$)
  - ***When di/dt>0***

$$i_{f_K}(t) = G_I\sin(\omega t - \gamma_I) + B_k\, e^{-\alpha^{I}t} \quad (4.13)$$

$$v_{C1_K}(t_k) = v_{C1_K}(t_{k-1}) = V_{C10_{k-1}} \quad (4.14)$$

  - ***When di/dt<0***

$$i^{II}_{f_K}(t) = G_{II}\sin(\omega t - \gamma_{II}) + e^{-\alpha^{II}t}\left(A_{1k}\cos|\beta|t + A_{2k}\sin|\beta|t\right) \quad (4.15)$$

$$v_{C1_K}(t_k) = \frac{1}{C_f}\int_{t_{k-1}}^{t_k} i_{f_K}(t_k)\,dt + V_{C10_{k-1}} \quad (4.16)$$

where

$$\alpha^{I} = \frac{R_f}{L_f}$$

$$G_I = \frac{V_m}{\sqrt{R_f^2 + (\omega L_f)^2}}$$

$$\gamma_I = \tan^{-1}\left(\frac{\omega L_f}{R_f}\right)$$

$$\alpha^{II} = \frac{R_f}{2L_f} \;\&\; \omega_0 = \frac{1}{\sqrt{L_f C_f}}$$

$$\beta = \sqrt{\omega_0^2 - \alpha^{II^2}}$$

A_{1k} & A_{2k} = constants

$$G_{II} = \frac{V_m}{\sqrt{R_f^2 + \left(\frac{\omega^2 L_f C_f - 1}{\omega C_f}\right)^2}}$$

$$\gamma_{II} = \tan^{-1}\left(\frac{\omega^2 L_f C_f - 1}{\omega C_f R_f}\right)$$

There are two important procedures that have to be applied during running the code:

- A_{1k} & A_{2k} should be recalculated at the end of each switching transition to be used as the initial conditions for the next state.

- The capacitor voltages have to be initialized at the beginning of each half cycle to the reference voltage (V_{cref}) to simulate the regulation circuit.

4.3.2 Parameters Estimation

The same procedure done in Section 3.4.2 is repeated here to get the optimum SC scheme parameters. The following observation is concluded from the optimization:

- The SC scheme performance has the same trend for the THD and switching frequency as the standard control strategy, i.e. the THD increases, switching

frequency decreases, with the increase in the inductor value and with small capacitor sizes.

- The source current THDs are less than their respective values in the standard control strategy. This is due to the improved performance of the SC scheme around area of zero crossings.
- The switching frequency is higher than the standard control strategy. This is because the area around the zero crossings has high switching frequency.
- The initial capacitor voltage is kept at the required level of 235 V, which allows more control of the choice of the passive elements and ensures that the capacitor voltage will be always higher than the peak of the supply voltage.

Finally, the parameters of the scheme are selected to be: inductor L_f = 3.0 mH (5%) and capacitor C_f = 260 uF (190%) that will result in a THD of 2.2% and a switching frequency of 2.8 kHz. Further, the capacitors will have an absolute minimum voltage V_{Cmin} of 203V, and an initial voltage V_{C0} of 235V.

4.4 Simulation Results

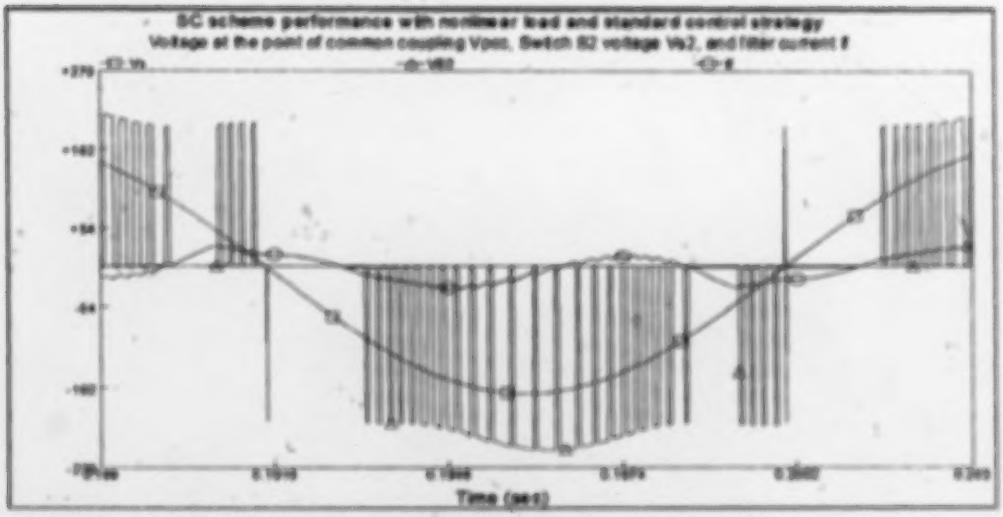
The validity of the performance of the modified control strategy is verified by means of simulation, with PSCAD, for both steady state and transient operations. The overall performance of the proposed power conditioner is evaluated in the next section with a laboratory prototype.

The case study is the same one used in the previous chapter: a SVC generating reactive power. Further, a non-linear load consisting of a diode bridge rectifier with a capacitive filter is simulated to investigate the effectiveness of the new control for harmonic mitigation. The waveforms for the power conditioner are done when operating with the modified hysteresis current control with a hysteresis window of 5.0% of the rated peak non-active current (i_{Lq}).

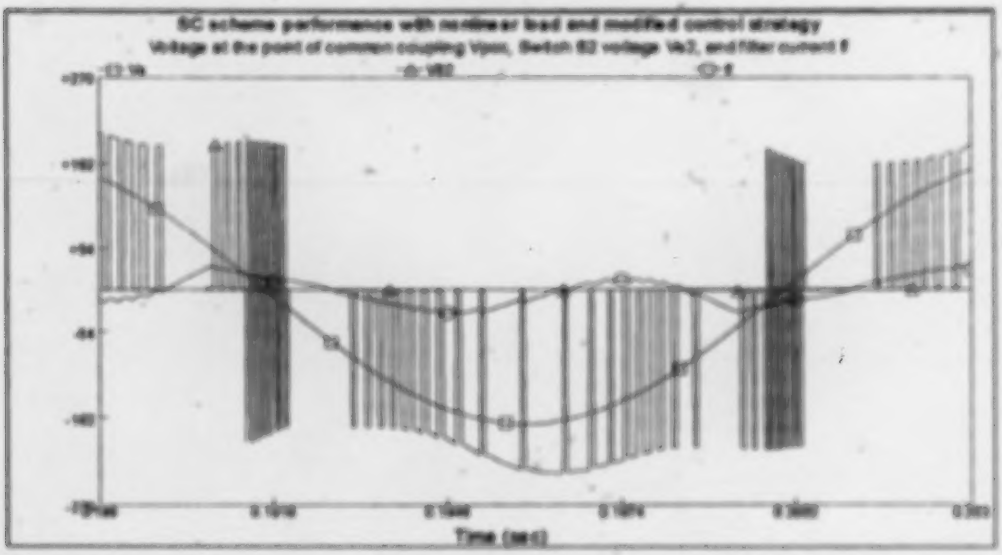
4.4.1 Steady State Operation

4.4.1.1 Comparison between switching instants of both standard and modified control strategies

One of the differences between the standard and modified strategies can be clarified from the comparison of the waveforms and switching instants in figure 4.6a and figure 4.6b, respectively, when the SC scheme is working as an active filter. On the one hand, the standard control has very few switching during the period of the zero crossings of the supply voltage as shown in figure 4.6a. On the other hand the modified control strategy could do multiple switching during the same period, as shown in figure 4.6b, to effectively track the required command current during this period. Therefore, by using the modified control circuit, the SC scheme should have an increased tracking capability for any command current more than in the case of using the standard control. Therefore, the source current THD should be improved and that will be confirmed when presenting the simulation results of the SC scheme when operating with non-linear loads.


SC scheme performance with nonlinear load and standard control strategy
Voltage at the point of common coupling Vpcc, Switch S2 voltage Vs2, and filter current If
Time (sec)

(a)


SC scheme performance with nonlinear load and modified control strategy
Voltage at the point of common coupling Vpcc, Switch S2 voltage Vs2, and filter current If
Time (sec)

(b)

Figure 4.6 (a) Window of i_S, v_{pcc}, *and* v_{S2} across the zero crossing of v_{pcc} with *standard* control strategy. (b) Window of i_S, v_{pcc}, *and* v_{S2} across the zero crossing of v_{pcc} with *modified* control strategy.

4.4.1.2 *Reactive power compensation*

Figures (4.7-4.10) present some relevant waveforms for the SC scheme when operating with linear loads. From the waveforms, it can be observed the following:

- Figure 4.7 shows the SC scheme performance when supplying capacitive current to the system, which has a lagging power factor of 0.75.

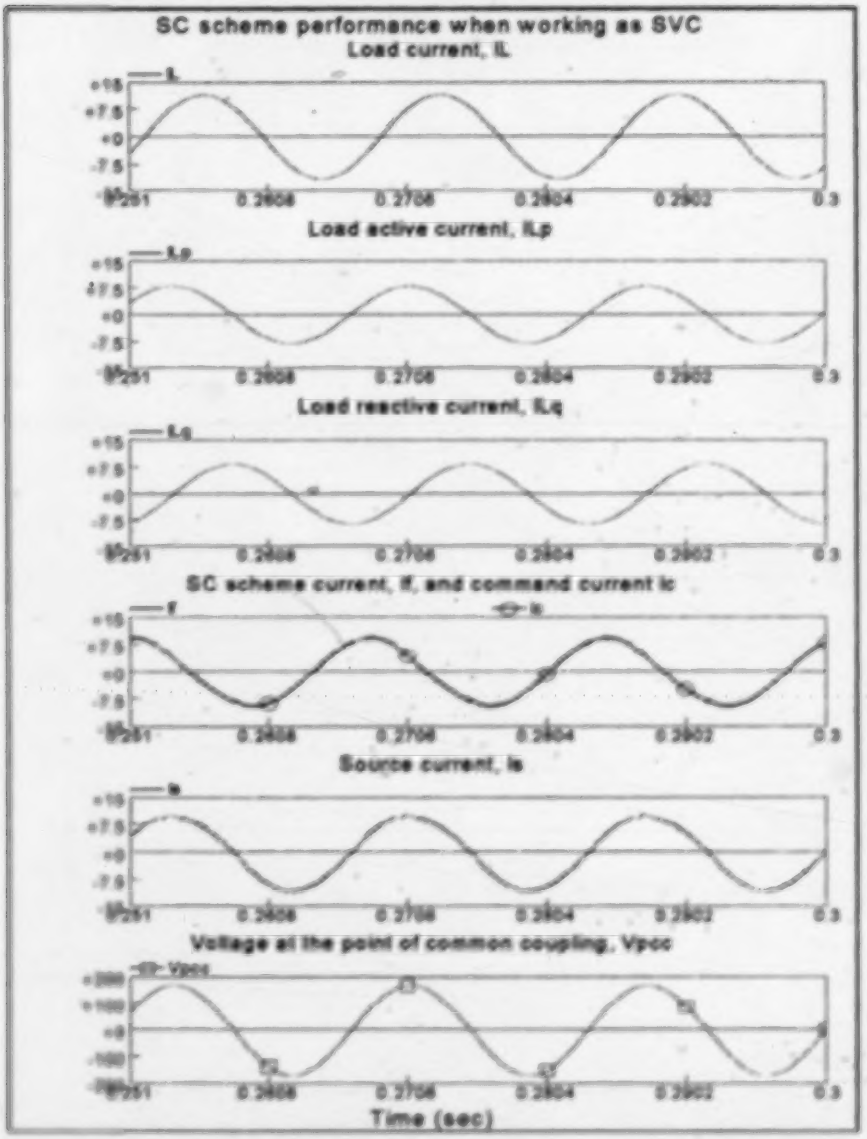
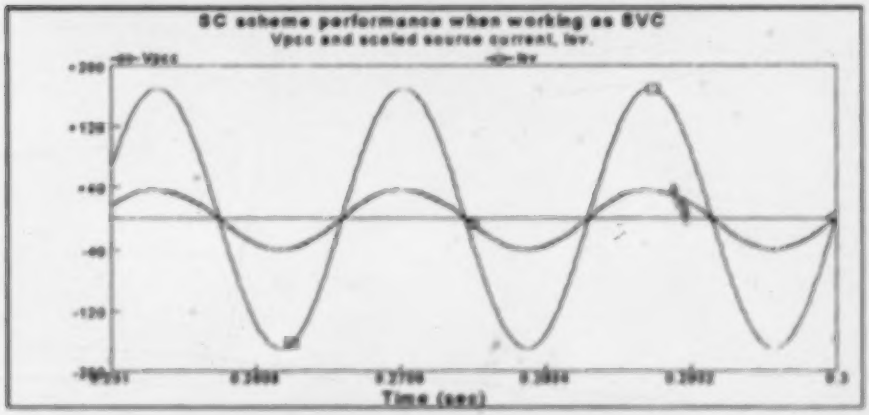
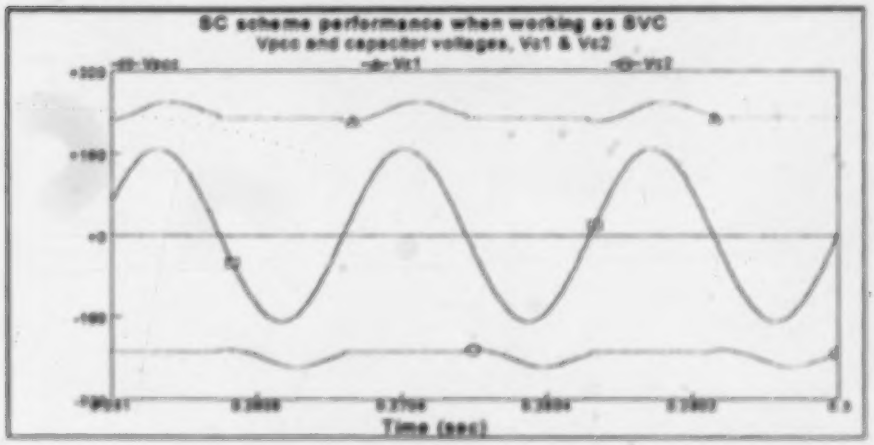

SC scheme performance when working as SVC
Load current, IL
Load active current, ILp
Load reactive current, ILq
SC scheme current, If, and command current Ic
Source current, Is
Voltage at the point of common coupling, Vpcc
Time (sec)

Figure 4.7 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c , and v_{pcc} for a linear inductive load.

- The figure further reveals that the modified control strategy could still effectively decompose the load current into its active and reactive components and provide the control circuit with the required reference current that enables the scheme to perform its function effectively that has been confirmed from the source current waveform.
- Further, the modified control strategy could correct the power factor to almost 1.0 that can be clarified in figure 4.8a.
- Using the voltage regulation loop could maintain the initial capacitor voltage at a level of almost 231 V as shown in figure 4.8b.



(a)



(b)

Figure 4.8 SC performance with an inductive load

(a) v_{pcc} and source current i_s.

(b) v_{pcc} and capacitor voltages and current (v_{c1} & v_{c2})

- The THD distortion in the source current is improved to be 3.0% instead of 3.8% at the case of the standard control strategy. This happens due to the new switching technique that increases the current tracking capability and the higher capacitor voltages that increases the rate of rise of SC scheme current. Finally, the system switching frequency increases from 2.1 to 2.4 kHz than the case of standard control strategy.
- Similar results for the SC scheme when supplying inductive current, worst case, to the system, which has a leading power factor of 0.74 is shown in figure 4.9.

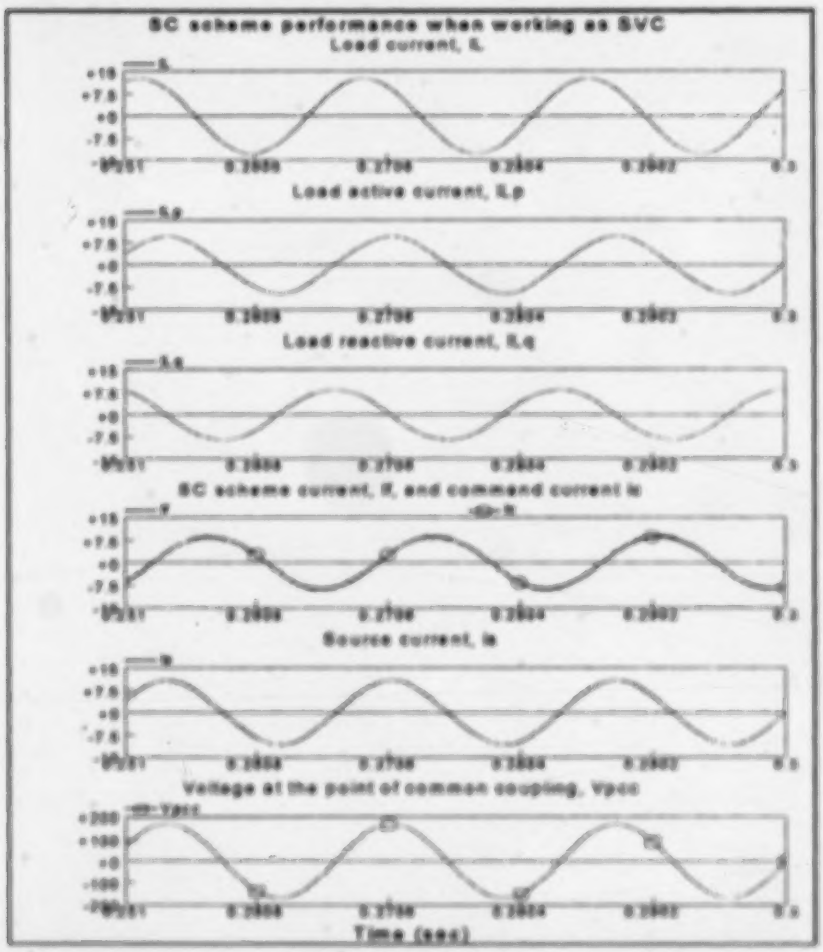
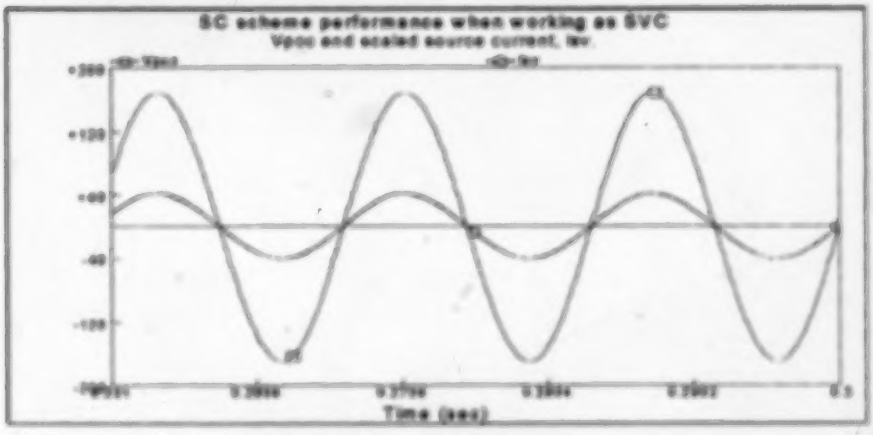
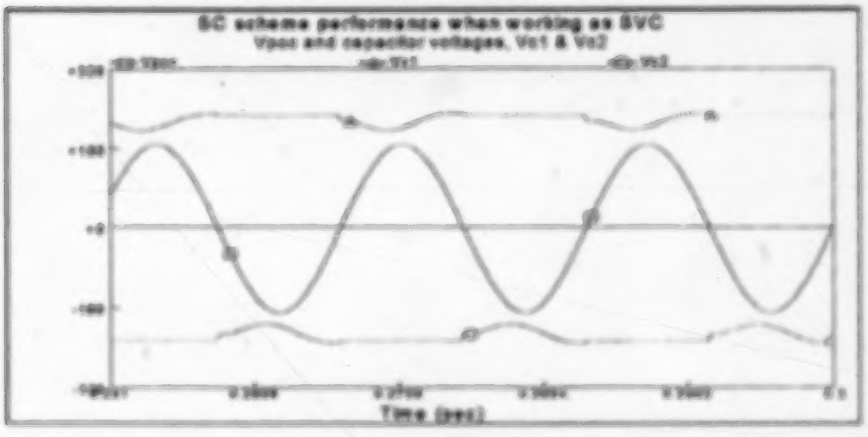

SC scheme performance when working as SVC
Load current, IL
Load active current, IL.p
Load reactive current, IL.q
SC scheme current, If, and command current Ic
Source current, Is
Voltage at the point of common coupling, Vpcc
Time (sec)

Figure 4.9 Load current, i_L, Load active current, $i_{L.p}$, and Load reactive current, $i_{L.q}$, Filter and command currents, i_f and i_c , and v_{pcc} for a linear capacitive load.

- The SC scheme could perform its function effectively by using the modified control strategy and correct the power factor to almost 1.0 that can be clarified in figure 4.10a.
- Using the voltage regulation loop could maintain the initial capacitor voltage at a level of 232 V that can be shown in figure 4.10b. Further, the SC power conditioner could perform its function effectively for the worst case condition, capacitive load, as the capacitor voltage has a ripple of almost 14% form the initial capacitor voltage, V_{Cmin} is 200, which ensure correct operation of the scheme.



(a)



(b)

Figure 4.10 SC performance with a capacitive load

(a) v_{pcc} and source current i_s.

(b) v_{pcc} and capacitor voltages and current (v_{c1} & v_{c2})

4.4.1.3 Harmonic mitigation

The performance of SC power conditioner with non-linear loads is presented in figures (4.11-4.13). The load under consideration is a diode bridge rectifier load with capacitor filter. From the waveforms, the following can be observed:

- There is an additional improvement in the source current waveforms and THD with the modified control strategy than the standard one as can be shown in the waveform of figure 4.11 and the spectrum of figure 4.12.

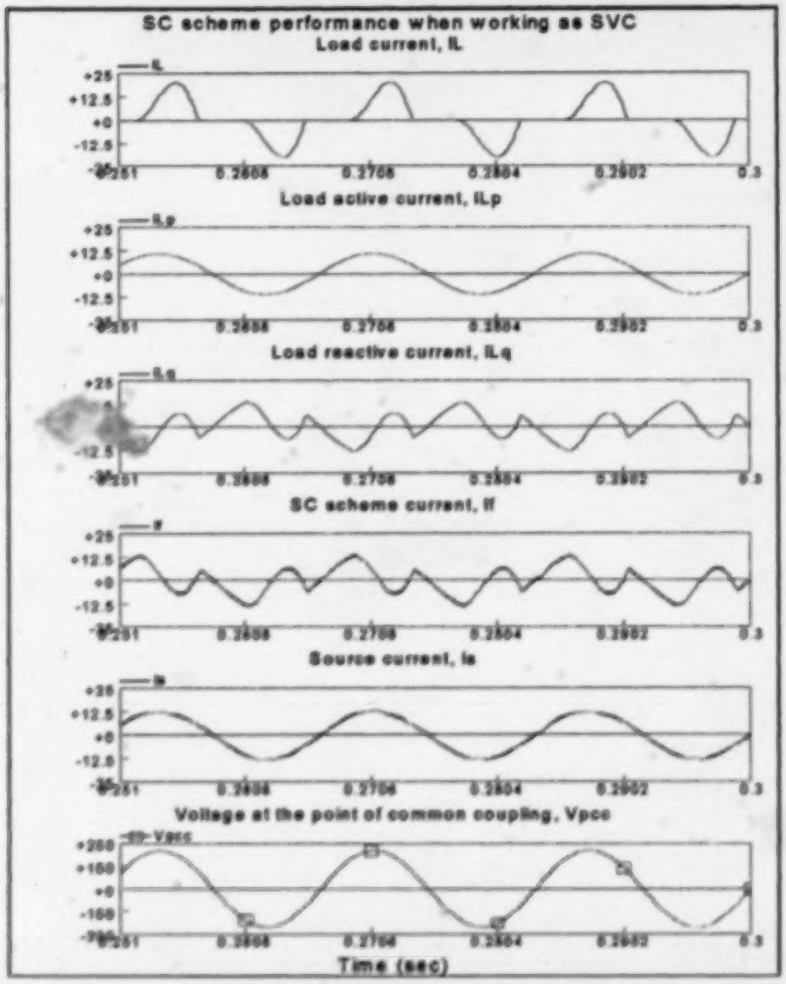

SC scheme performance when working as SVC
Load current, IL
Load active current, ILp
Load reactive current, ILq
SC scheme current, If
Source current, Is
Voltage at the point of common coupling, Vpcc
Time (sec)

Figure 4.11 Load current, i_L, Load active current, i_{Lp}, and Load reactive current, i_{Lq}, Filter and command currents, i_f and i_c , and v_{pcc}, for a diode bridge rectifier with capacitor filter load.

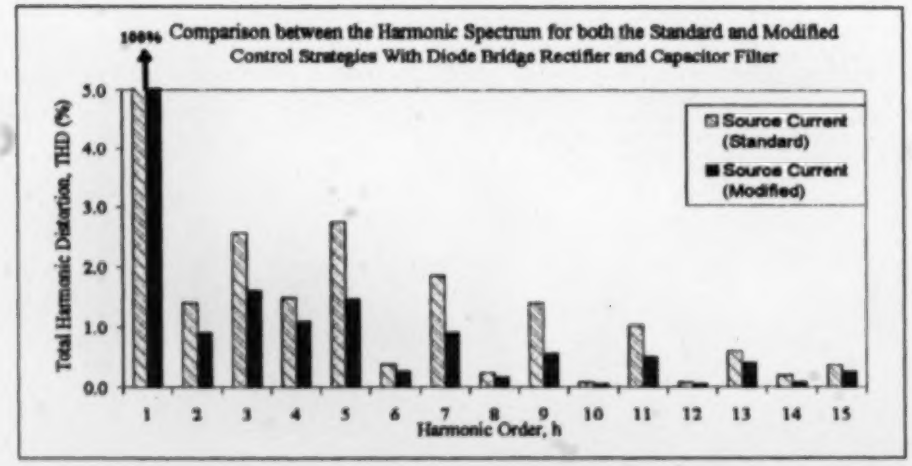
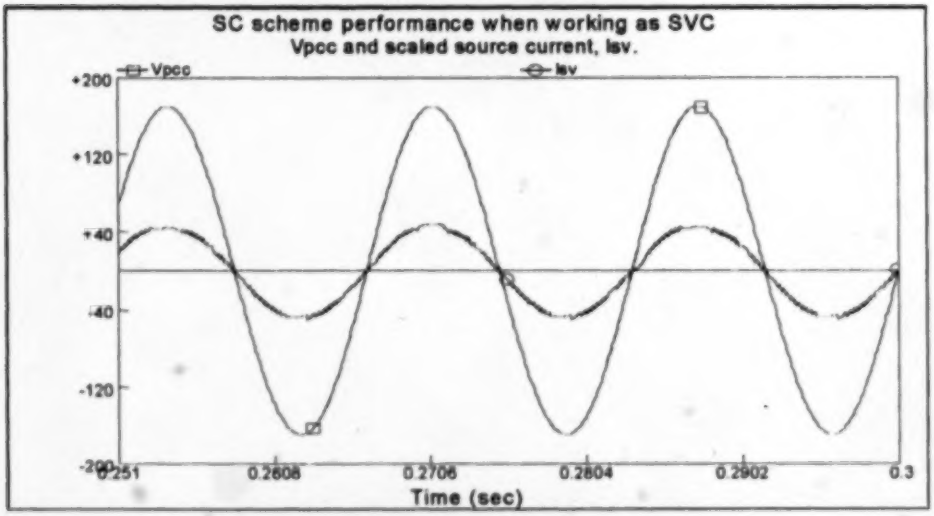

100%
Comparison between the Harmonic Spectrum for both the Standard and Modified Control Strategies With Diode Bridge Rectifier and Capacitor Filter
Source Current (Standard)
Source Current (Modified)
Total Harmonic Distortion, THD (%)
5.0
4.0
3.0
2.0
1.0
0.0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Harmonic Order, h

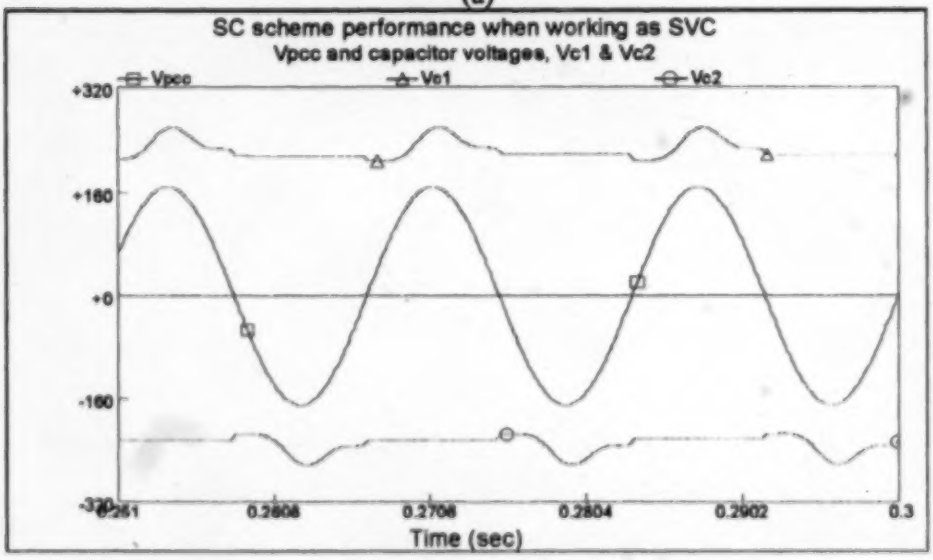
Figure 4.12 Comparison between the harmonic spectrum for both the standard and modified control strategies with diode bridge rectifier and capacitor filter.

- The THD could be improved from 7.7% with standard hysteresis control to 4.2% with the modified control strategy.
- Further, from the spectrum, one can see that using the modified control strategy can reduce the odd individual harmonic components with 30 to 50% of their respective components in the standard one.
- The modified control strategy could correct the power factor from 0.65 to almost 0.98 as shown in figure 4.13a.
- Although, further attenuation in THD using the standard hysteresis is difficult to achieve mostly due to the small voltage available to increase (decrease) the filter current during zero voltage crossings of the PCC voltage. In principle the THD attenuation using the modified control strategy could be further improved by increasing the region where S_2 and S_3 switch but it has to be limited to around 15% of the maximum supply voltage when the capacitor voltage starts to present a very large ripple and to reduce the switching losses during the whole operation. It is worth mentioning that the SC scheme could achieve its performance with a switching frequency of 3.6 kHz that may change depending on the type of the load used in the simulation.

- Finally, Using the voltage regulation loop could maintain the initial capacitor voltage at a level of 231 V with a minimum capacitor voltage of 223 V and maximum capacitor voltage of 254V as can be shown in figure 4.13b.



(a)



(b)

Figure 4.13 SC performance with an inductive load,

(a) v_{pcc} and source current i_s.

(b) v_{pcc} and capacitor voltages and current (v_{c1} & v_{c2})

4.4.2 Transient Analysis

This section discusses the performance of the SC compensator under different transient conditions. Simulation results are presented to demonstrate the speed of response of the proposed compensator when working with the modified control strategy.

4.4.2.1 Reference current variation

Figure 4.14 shows the response of the switched capacitor based compensator when the reference current changes in a step-like manner from 1.0 p.u. to 0.75 p.u and back to 1.0 p.u. in a period of 0.3 s.

There one can see that the proposed scheme is effective in tracking the required reference current for both cases with a fast dynamic response. For rated and reduced capacitive reference current, as shown in figure 4.14a, the measured values for initial capacitor voltage V_{C0} has a minor change from 231V to 229 V and this is due to the fast response of the scheme that allows a very small active current to flow. However, the voltage ripple has some visible change as V_{max} varies from 255V to 247V respectively which is a factor of current magnitude and capacitor size.

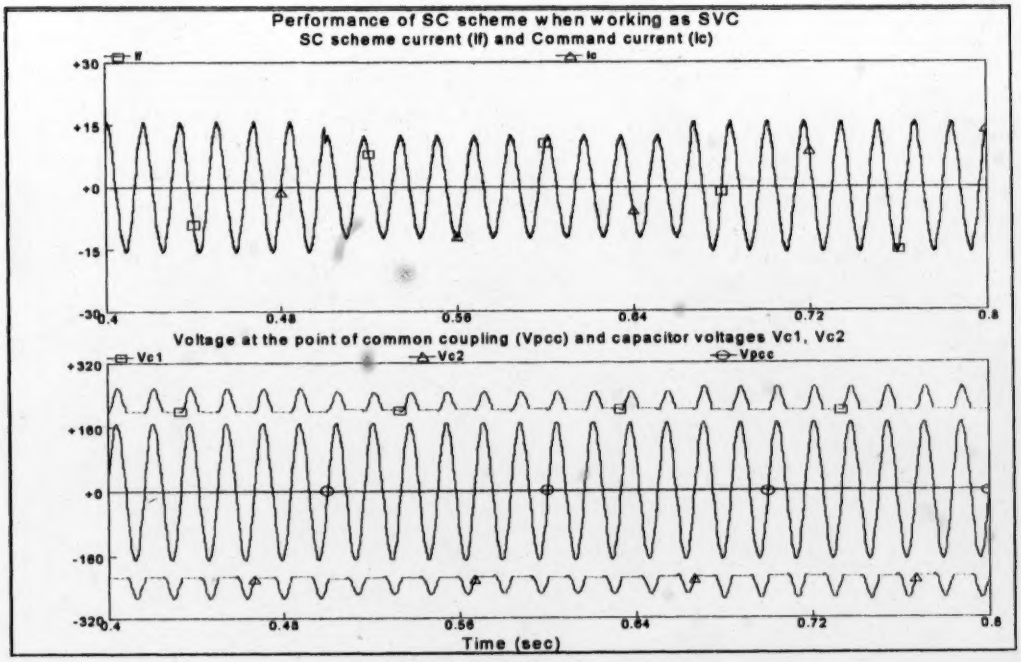
For rated and reduced inductive reference current the measured values for V_{C0} and V_{min} were 232 V and 207-213V respectively. The results were obtained for a reference inductive current as shown in figure 4.14b.

Finally, it is worth mentioning that the minimum capacitor voltage is close to the peak of the supply voltage for certain current magnitudes and careful design procedure for the scheme elements should be done to avoid any system instability.

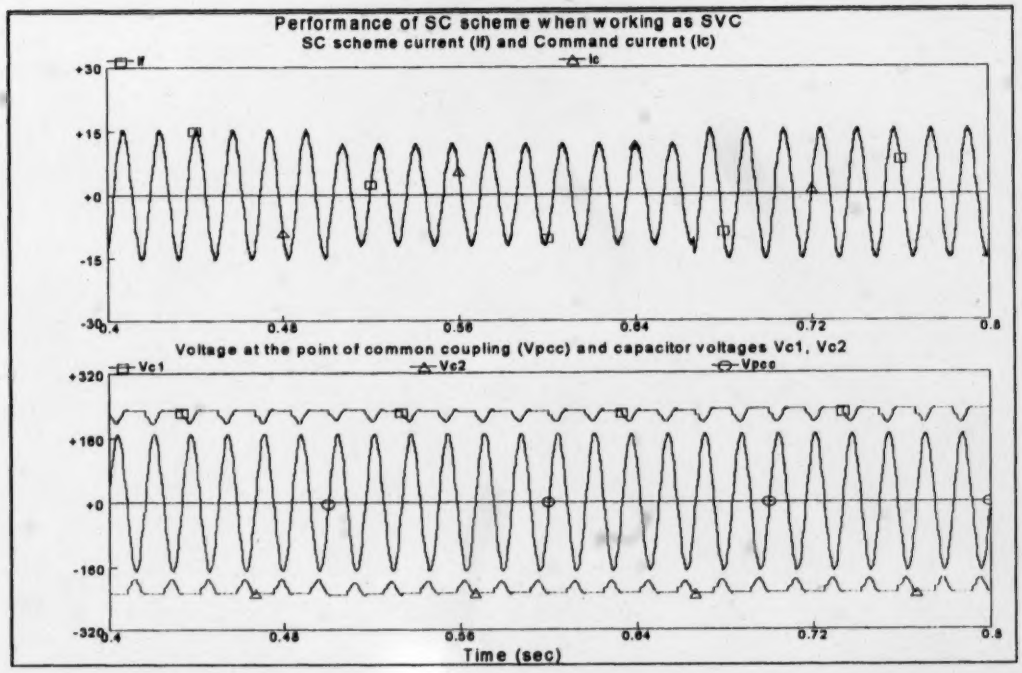
4.4.2.2 Supply voltage variation with constant current

In this test, the switched capacitor compensator operates as a SVC with rated (10A) reference current that can be either capacitive or inductive.

For the results presented in figure 4.15, the 60 Hz ac mains voltage magnitude varies from 120 to 100 V with a 3.0 Hz frequency.

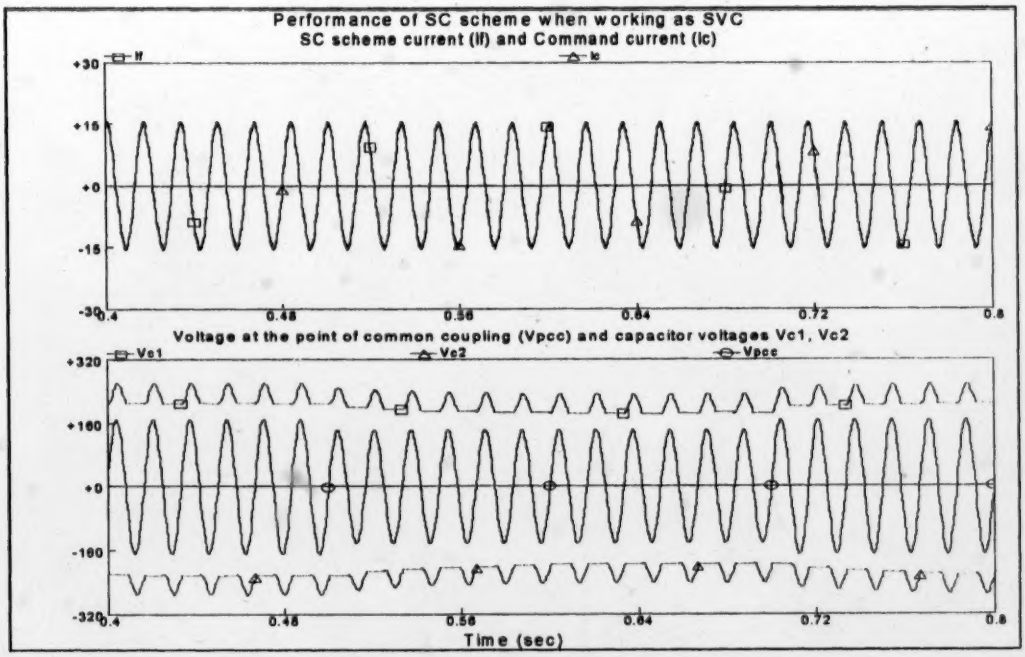


(a)

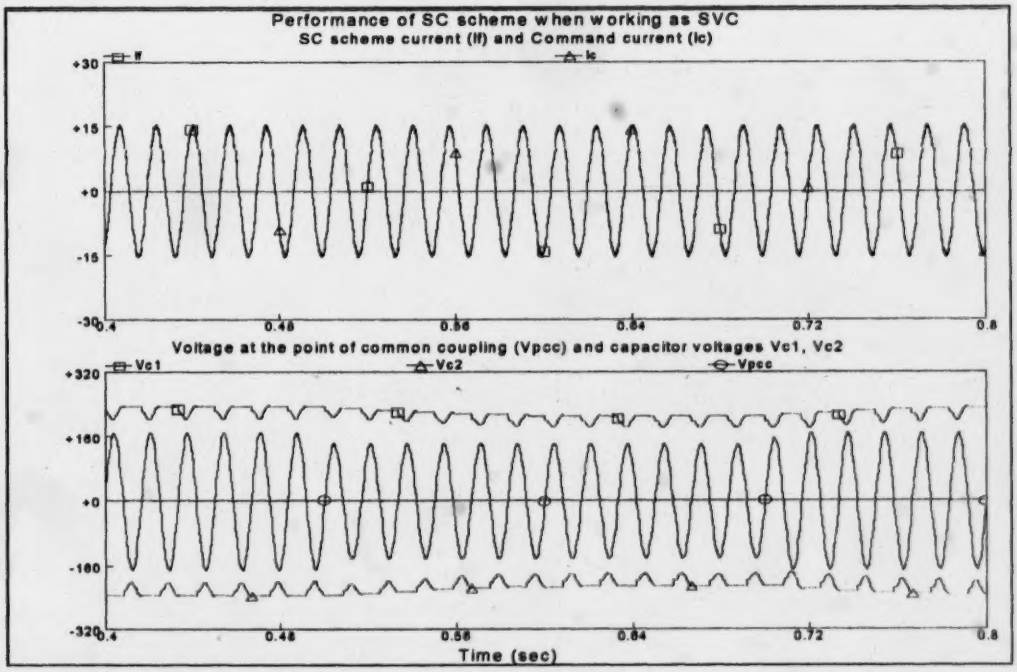


(b)

Figure 4.14 Response of the SC scheme with a step change in the reference current for: (a) Reference capacitive current (b) Reference inductive current.



(a)



(b)

Figure 4.15 Response of the SC scheme with a step change in the voltage for:

(a) reference capacitive current (b) Reference inductive current.

There one may observe, for both inductive and capacitive reference currents, that the actual current sticks to the reference.

Unlike the standard thyristor based SVCs, the proposed compensator should be able to deliver rated (maximum) capacitive current during voltage sags. One can see from figure 4.15a that the capacitor voltage starts to decrease and stabilizes at a value below the reference one. This happens due to the fixed proportional controller, K_{12}, in the capacitor voltage loop. However, one can see from the simulation, that SC scheme could still perform its function and provide a current that maintain a sinusoidal supply current that in phase with the voltage. Thanks to the voltage regulation loop the capacitor voltage changes proportionally to the supply voltage.

Therefore, the capacitor voltage in this situation will always remain higher than the supply voltage that allows the SC scheme to perform it operation properly and in a fast manner as seen in figure 4.15a.

Figure 4.15b simulates the previous case, sag, but with a reference inductive current. The capacitor voltage has the same trend as the previous case and tends to decrease with the voltage sag. However, due to the inertia of the capacitor, the voltage was varying slowly with the change in supply voltage. Depending on the magnitude of the voltage sag, the capacitor voltages can become smaller than the peak value of the mains voltage, what can result in some distortions in the SVC current. Besides, during the return of the supply voltage to its rated value, the reference current generating circuit tends to increase the magnitude of the reference current which further reduces V_{Cmin}. One possible solution is to have reference voltage that changes with supply voltage to keep a constant capacitor voltage for any supply voltage changes.

Conversely, if a swell takes place in the ac mains, not shown, operation with rated inductive current would be trouble-free while operation with rated capacitive current would result in an increased voltage stress across the power switches. Therefore, the proposed compensator can still supply rated capacitive current, provided that the power switches are designed to withstand the increased voltage stress.

4.4.2.3 Supply voltage variation with constant reactive power

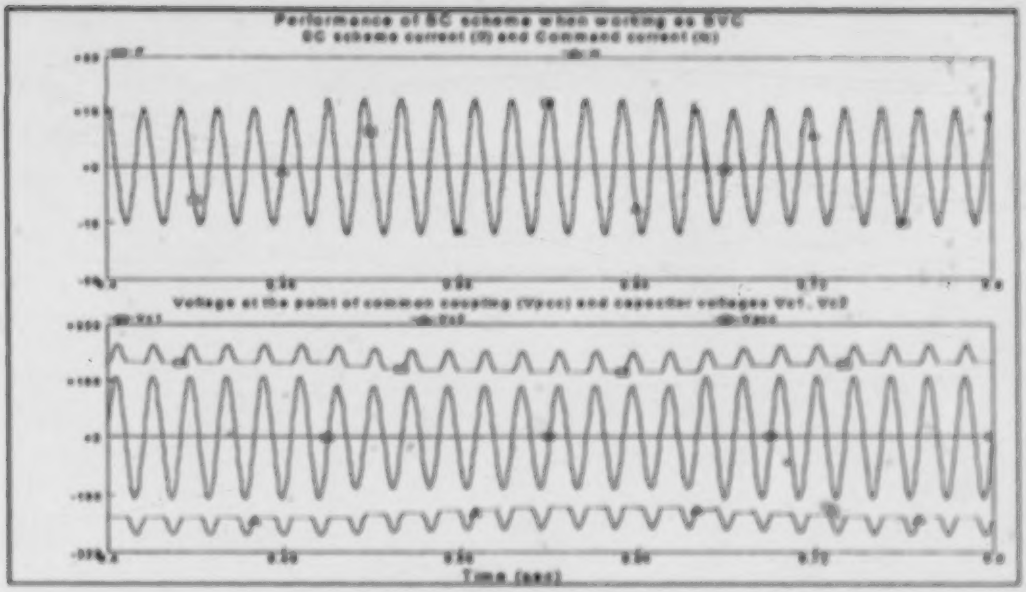
A constant reactive power that can be achieved by simultaneous change in the voltage (decrease) and current (increase) or vice versa is investigated in figure 4.16a,b. The ripple in the capacitor voltage starts to be bigger than the one described in figure 4.15a,b because of the higher current magnitude. However, by using the systematic design approach, the value of the inductor and capacitor could be adjusted to cope with a given voltage variation. Further, the capacitor has some inertia that slows the rate of voltage variation. A major advantage of this type of converter is that the maximum reactive power decreases linearly with the mains voltage instead of with the square value as in variable reactance type compensators.

4.4.2.4 Variation of the load power factor

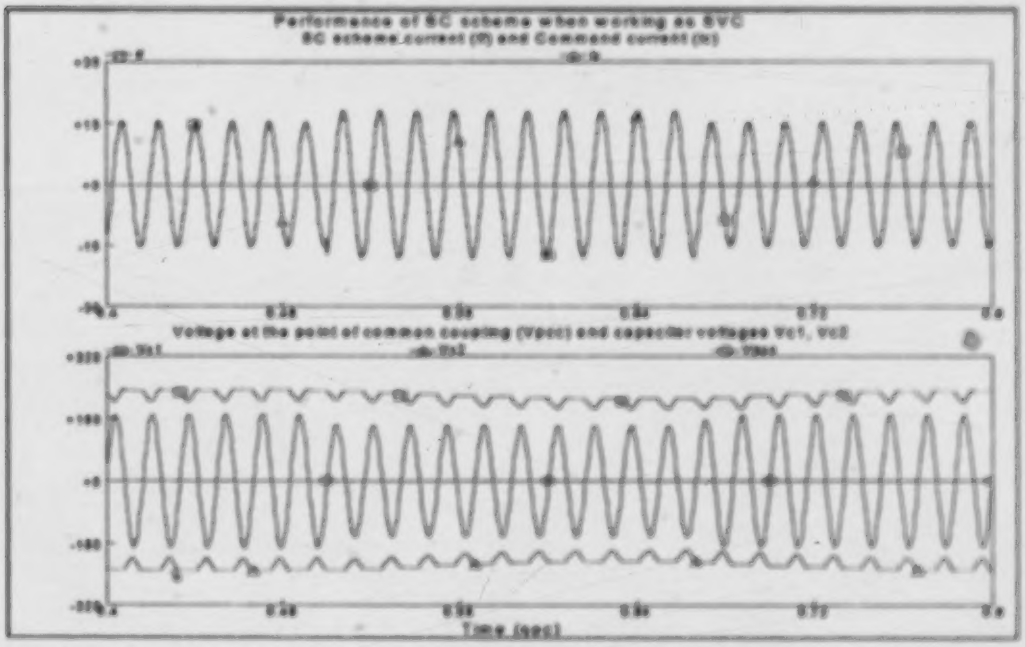
This test is concerned with the performance of the switched capacitor based SVC to compensate for sudden variations of the reactive power drawn by a linear load, yielding unit power factor.

The circuit depicted in figure 4.17 generates the reference current. It is assumed that a 1.5 kVA load operates initially with a 0.866 lagging power factor which changes suddenly to 0.866 leading and then back to 0.866 lagging power factor.

One may see that the reactive current (i_{LQ}) of the load can be effectively extracted by using the circuit depicted in figure 4.17. The figure also shows that the current injected in the ac mains by the power conditioner (i_f) follows closely the command current (i_c) and that it yields almost total compensation of the reactive power drawn by the load, with an increase in the total power factor from 0.866 to 1.00. The results further show that the scheme could respond to the change in the current within almost half a cycle. Further, the capacitor voltage loop is able to change the SC scheme capacitor voltage in a fast manner to compensate for this sudden change.


Performance of SC scheme when working as SVC
SC scheme current (Ic) and Command current (Ic)
Voltage at the point of common coupling (Vpcc) and capacitor voltages Vc1, Vc2
Time (sec)

(a)


Performance of SC scheme when working as SVC
SC scheme current (Ic) and Command current (Ic)
Voltage at the point of common coupling (Vpcc) and capacitor voltages Vc1, Vc2
Time (sec)

(b)

Figure 4.16 Response of the SC scheme with a step change in both the supply voltage and reference current for: (a) Reference capacitive current (b) Reference inductive current.

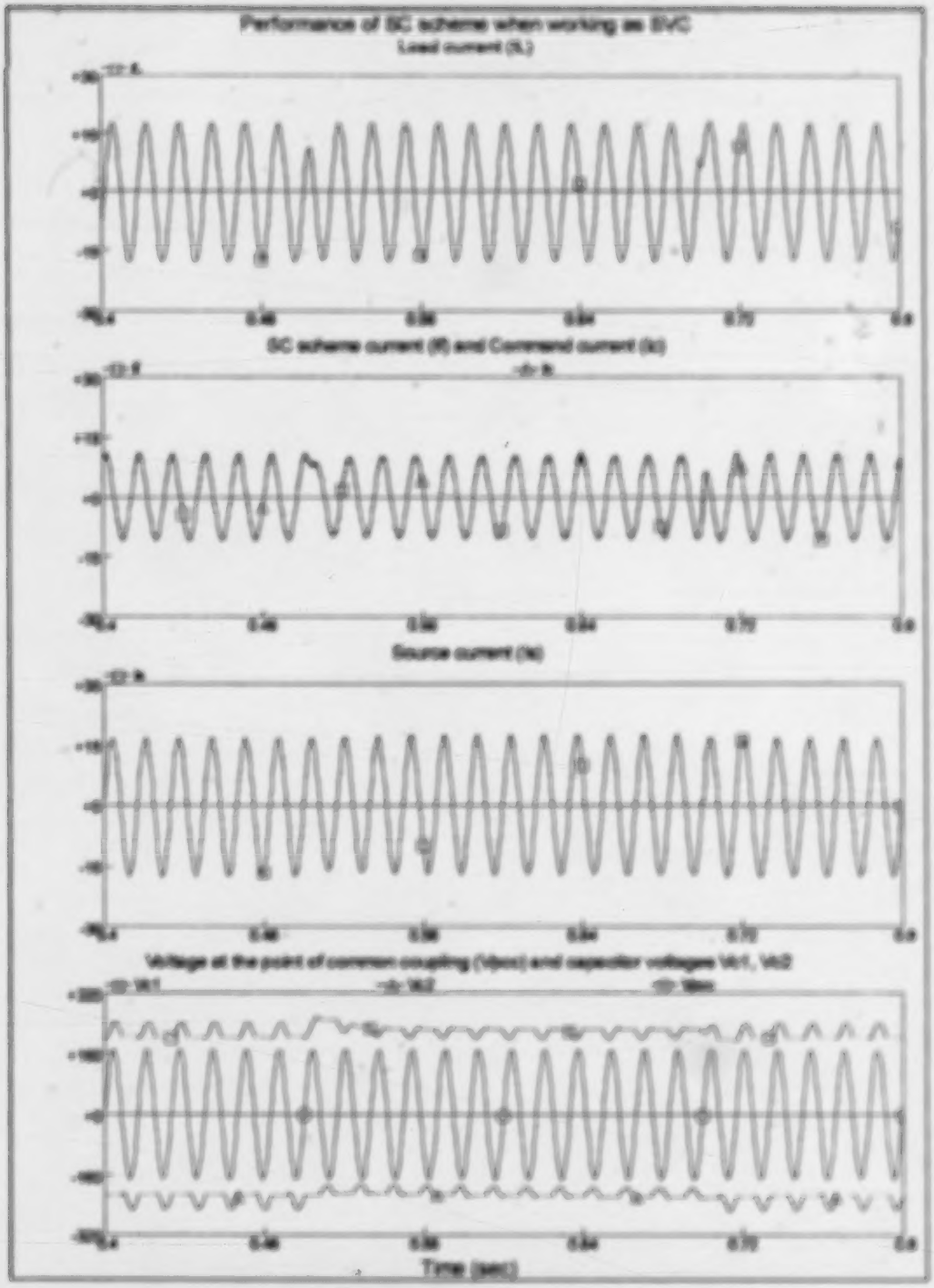

Performance of SC scheme when working as SVC
Load current (IL)
SC scheme current (If) and Command current (Ic)
Source current (Is)
Voltage at the point of common coupling (Vpcc) and capacitor voltages Vc1, Vc2
Time (sec)

Figure 4.17 Response of the SC scheme with a step change in the power factor of 1.5 kVA load from 0.866 lagging to 0.866 leading.

4.4.2.5 Variation of a non-linear load

As mentioned earlier, the proposed switched capacitor-based power conditioner can compensate for reactive power and also mitigate current harmonics. This is a very important feature for the compensation of thyristor based ac-dc converters that operate with variable loads and firing angles and which can create flicker or trigger resonances in the power system. Figure 4.18 presents some waveforms related to the compensation of a thyristor bridge rectifier with an inductive load, L_{dc} = 50.0 mH, R_{Load} = 5.0 Ω when the firing angles varies from 15° to 30° and back to 15°.

The reference current generating circuit is able to separate the non-active from the active component of the load current as shown in the figure. The scheme could respond faster than the previous case, linear load, due to the slow response of the Thyristor Bridge to the change in the firing angle.

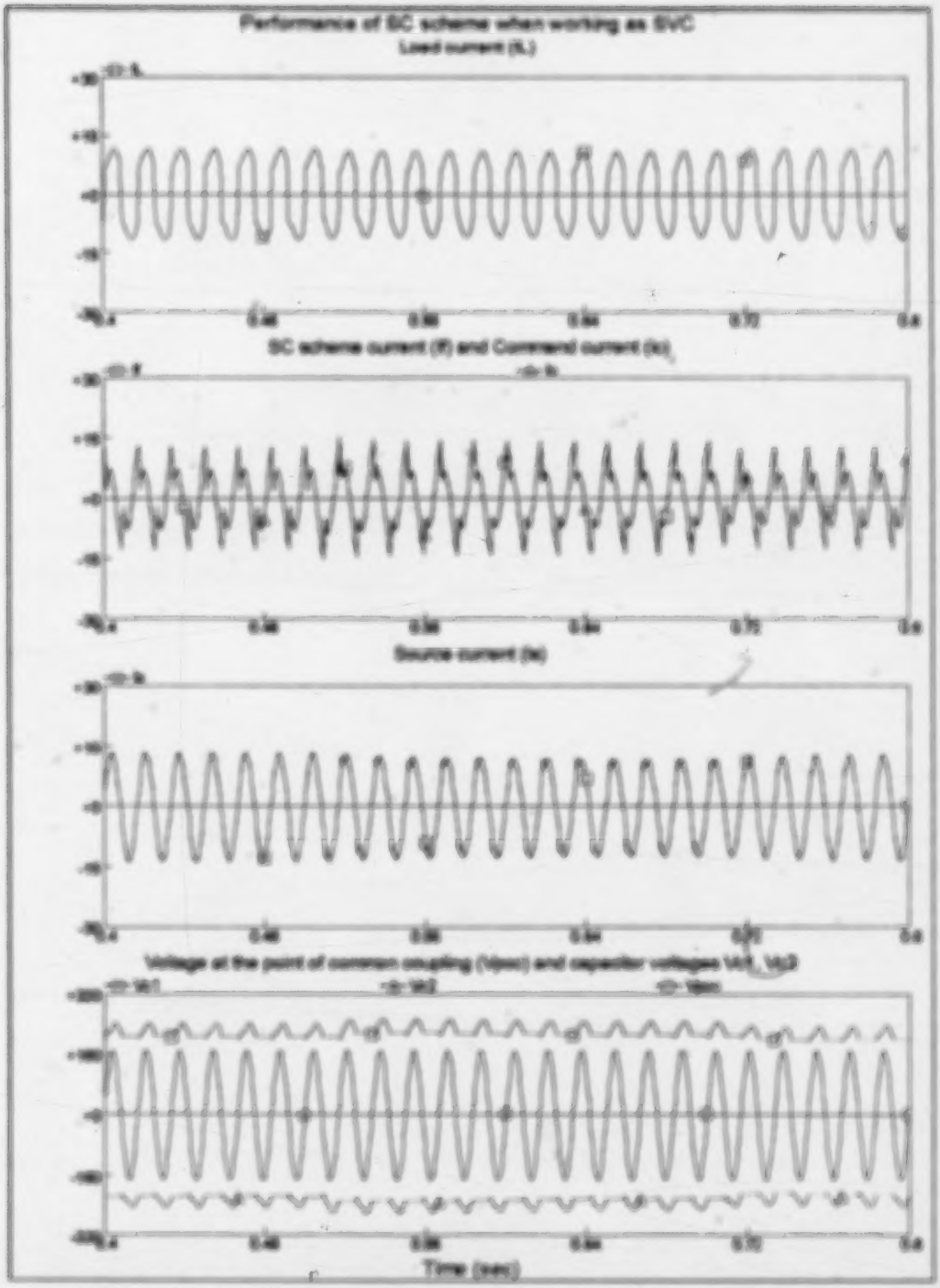

Performance of SC scheme when working as SVC
Load current (IL)
SC scheme current (If) and Command current (Ic)
Source current (Is)
Time (sec)

Figure 4.18 Response of the SC scheme with a step change in the firing angle thyristor bridge rectifier with an inductive load, L_{ab} = 50.0 mH, R_{Load} = 5.0 Ω from 15° to 30°.

4.5 Experimental Set up

A hardware model was built to confirm the simulation results and to verify the effectiveness of the modified control strategy. The circuit was built as the circuit diagram in figure 4.5. The current set up uses some of the circuits that were used in the Section 3.5 such as the power circuit, voltage and current sensing circuits, dead time circuit, and driving circuit. Finally, experimental waveforms will illustrate the performance of the laboratory set-up under different load conditions.

4.5.1 Control Circuit

Figure 4.19 shows the schematic diagram of the control circuit hardware. It consists of five main sub circuits:

- ***Capacitors voltage regulation loop sub circuit***: that is designed according to the analysis done in Section 4.2.2.
- ***Hysteresis comparator sub circuit***: the circuit that compares between the command current and actual filter current to get the switching signal, OUT_1, that controls the three switches S_1, S_2, and S_3.
- ***Voltage zero crossing detector sub circuit***: this circuit is used to provide the control circuit with the moment, OUT_2 shown in the figure, to change control from positive cycle to negative cycle.
- ***Positive and Negative level detectors sub circuit***: the circuit that compares between the voltage at the point of common coupling v_{pcc} and a positive and negative dc levels to get a period around the zero crossing of the voltage to effectively track the command current. This period is defined by the two outputs OUT_3, and OUT_4.
- ***Logic Circuit***: the four outputs, OUT_1, OUT_2, OUT_3, and OUT_4, are provided to the logic circuit of the modified control strategy that is constructed as shown in Fig 4.20. The outputs from the logic circuits are the signals to three switches S_1, S_2, and S_3.

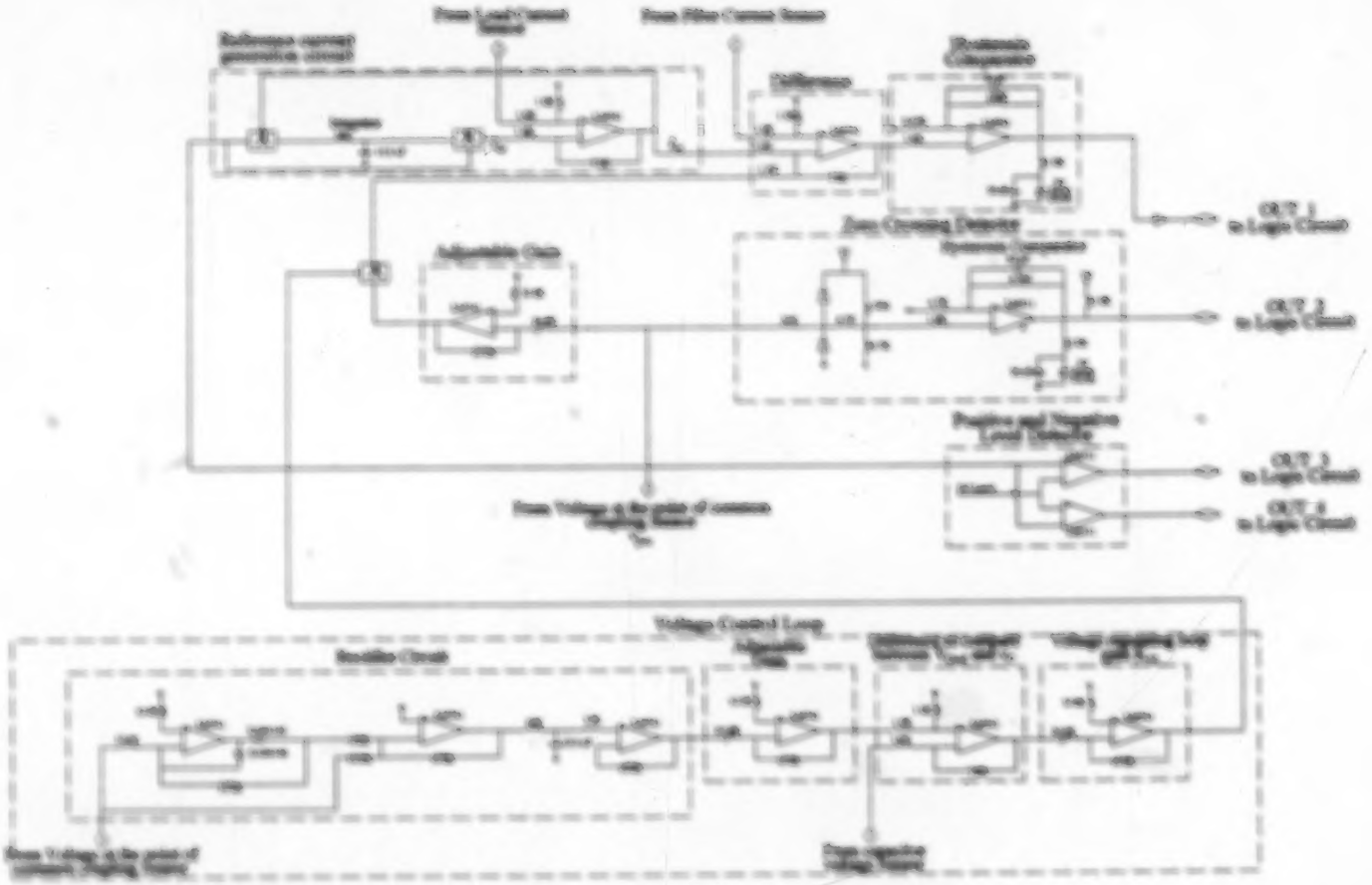


Figure 4.19 Control circuit hardware for reactive power compensation

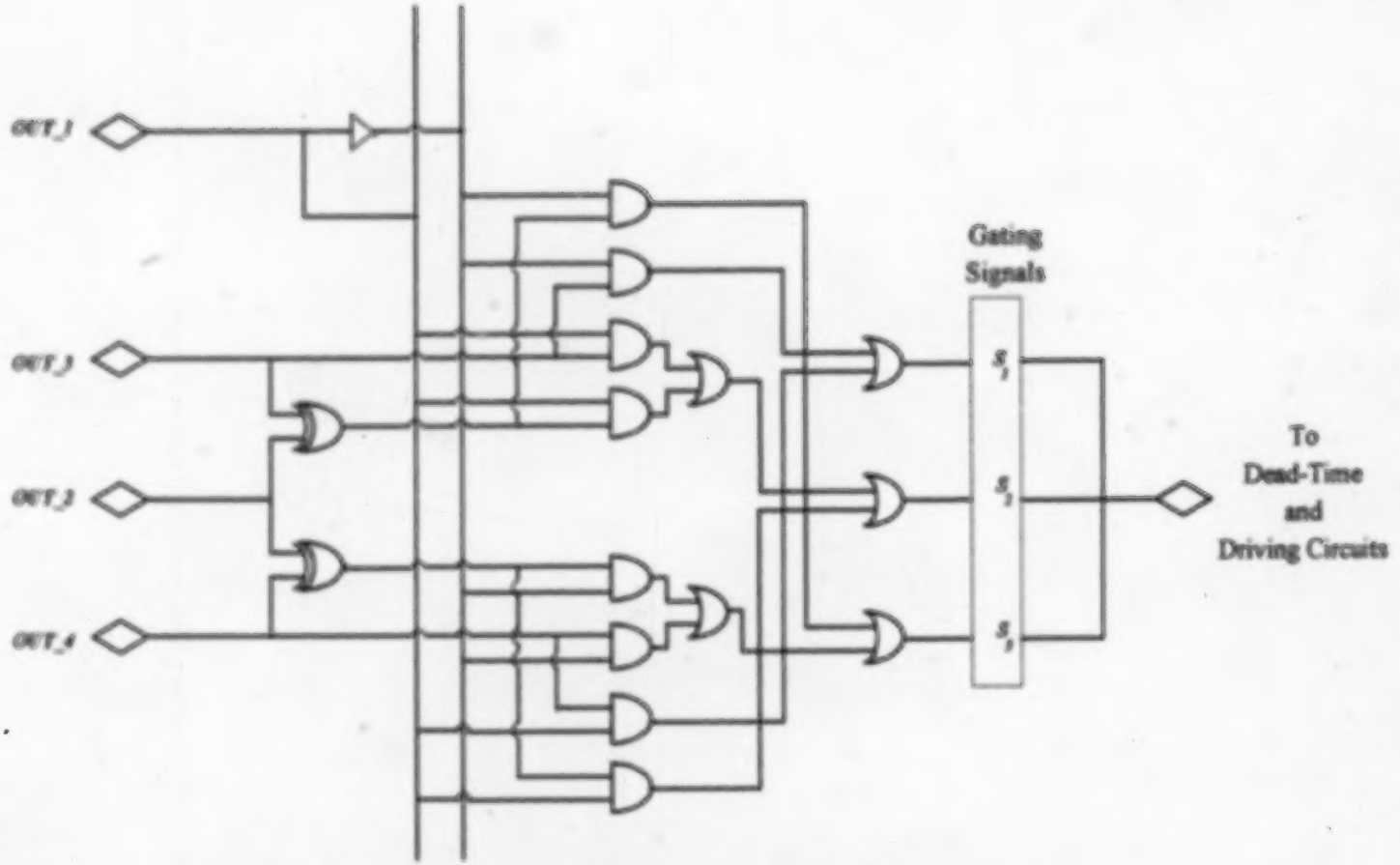


Figure 4.20 Experimental set up of the logic circuit of the modified control strategy.

4.5.2 Experimental Results

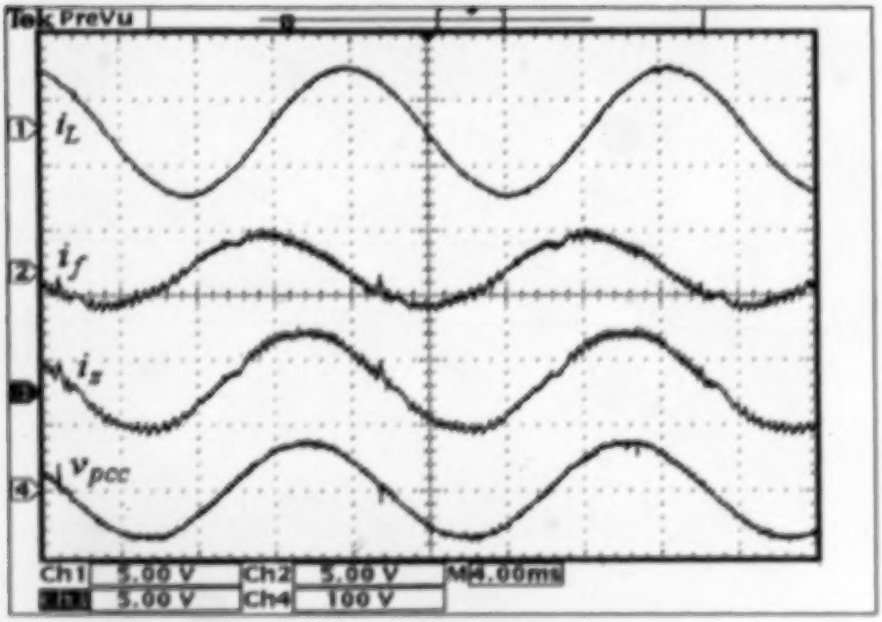
4.5.2.1 Reactive power control

The waveforms in Fig 4.21a,b illustrate the operation of the SC scheme for reactive power compensation of an inductive and a capacitive load respectively. The specification of the SC compensator, source and load are as follows:

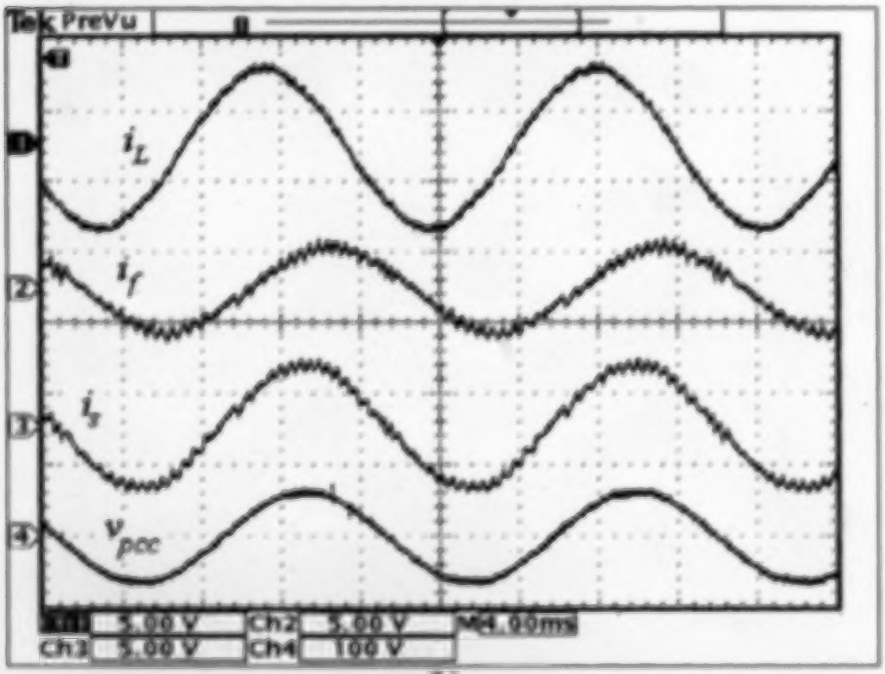
- Utility system: A regulated single-phase ac supply of 120 Vrms, 60 Hz; Line resistance, R_s=0.1 Ω, Line inductance, L_s=0.1 mH.
- SC VAR compensator: L_f = 3.0 mH, C_f = 260.0 μF.
- Load: Inductive load, L= 24 mH, R = 10.0 Ω , Capacitive load, C= 340.0 μF, R = 10.0 Ω

The load current (i_L), power conditioner current (i_f), supply current (i_s), and supply voltage (v_s) are shown in these figures. It can be seen from the waveforms that the power conditioner generates currents that are 90° leading, figure 4.21a, or 90° lagging, figure 4.21b, with respect to its supply voltage, as predicted.

Their magnitudes are such that the source current is almost in phase with the source voltage yielding an almost unity total power factor at the PCC. In fact the power factor improved from 0.74 lagging to 0.99 in the first case and from 0.78 leading to 0.99 in the second case. The supply current presents mostly high frequency harmonics and a THD of 4.1% and 3.7% for both cases respectively. It is worth mentioning that the proposed power conditioner achieved reactive power compensation with low harmonic distortion despite an average switching frequency of only 2.5 kHz as shown in figure 4.22. An even lower THD can be obtained by decreasing the hysteresis window at the expense of higher switching losses. The capacitor voltage waveforms, v_{c1} and v_{c2}, along with the supply voltage and power conditioner current are shown in figure 4.23 for the inductive load case. The initial and peak values of the capacitor voltages are 75V and 82V, which meet the design specifications.



(a)



(b)

Figure 4.21 Load current, power conditioner current, supply current and voltage at the point of common coupling respectively with (a) inductive load (L = 24 mH, R = 10 Ω), (b) capacitive load (C = 340 uF, R = 10 Ω).

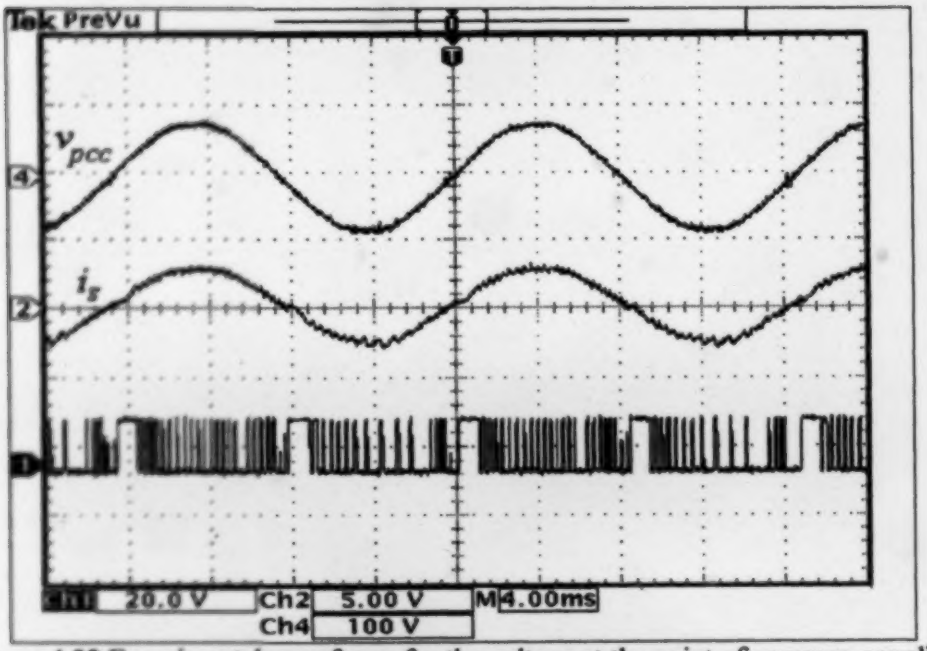


Figure 4.22 Experimental waveforms for the voltage at the point of common coupling v_{pcc}, supply current i_s, and switching signals.

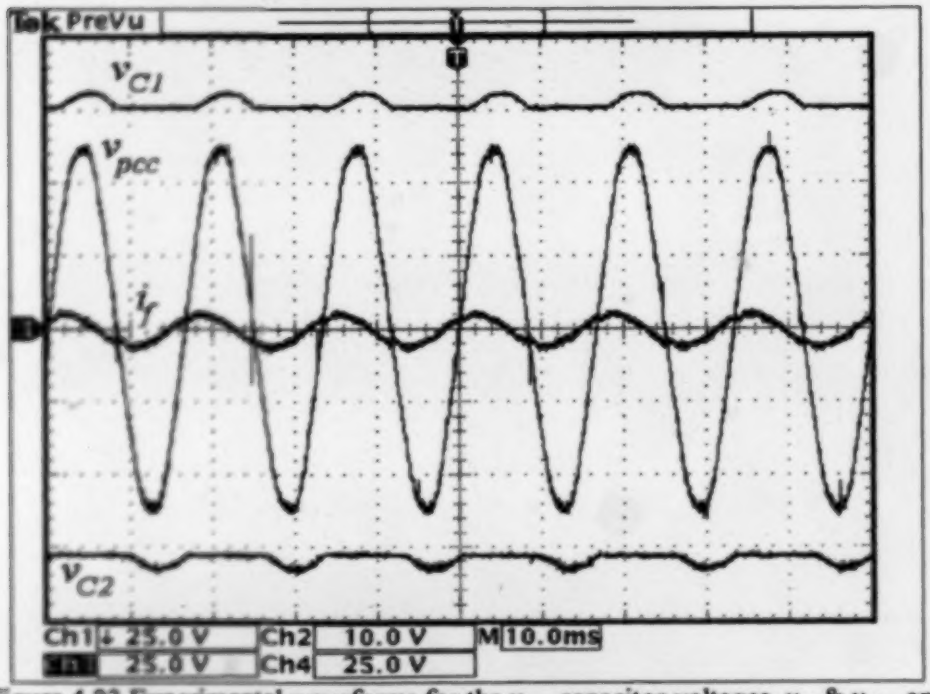


Figure 4.23 Experimental waveforms for the v_{pcc}, capacitor voltages, v_{c1} & v_{c2}, and power conditioner current i_f for a capacitive reference current.

4.5.2.2 Harmonic mitigation and reactive power control

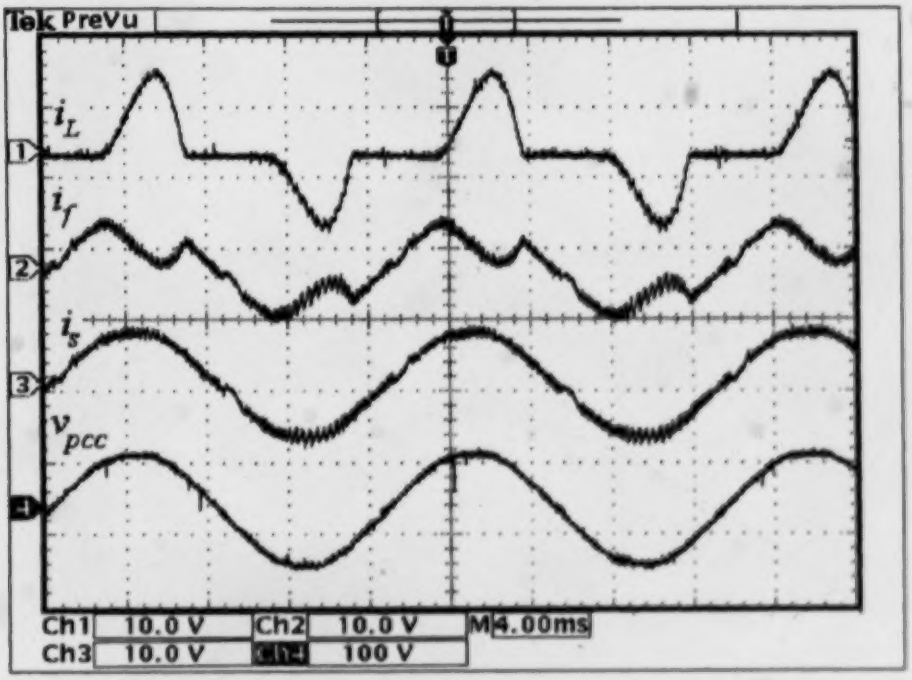
The proposed power conditioner was also evaluated for compensating common non-linear loads such as single-phase diode rectifiers with either inductive or capacitive dc filters. The rectifiers usually present a series reactor in the ac side to reduce the injected current harmonics that result in a lagging displacement power factor. Figures (4.24-4.25) show that the proposed power conditioner can compensate for the current harmonics and reactive power at the same time.

A 5.0 % reactor is used in the ac side of a diode bridge rectifier with either one of the following:

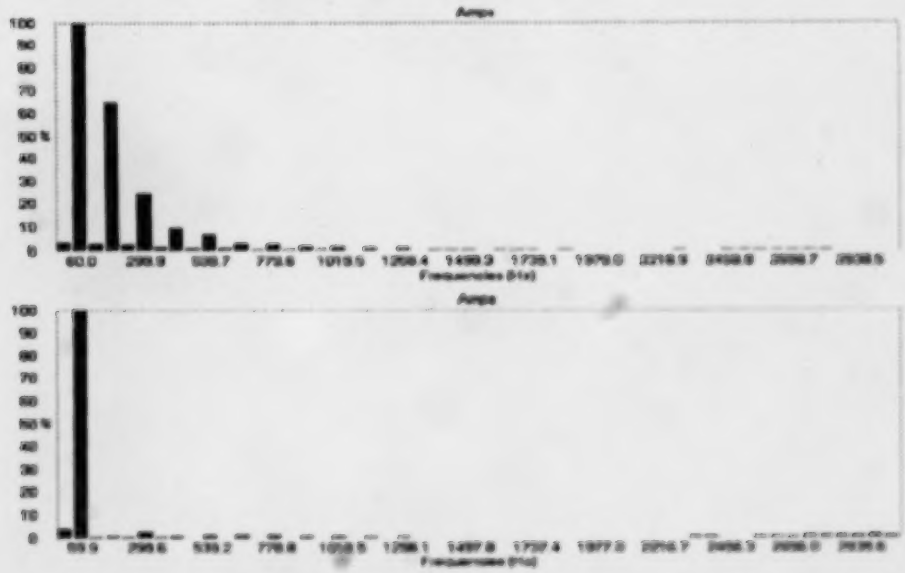
- A capacitor filter, C_{dc} = 940.0 μF, R_{Load} = 22.0 Ω.
- An inductive load, L_{dc} = 50.0 mH, R_{Load} = 5.0 Ω

Figure 4.24a shows the waveforms of the load current, power conditioner current, source current, and supply voltage for a single-phase rectifier bridge with a capacitive filter. The THD of the input current of the rectifier (i_L) is 58%. The power conditioner reduces the THD of the source current to 4.4%, when using the modified control strategy, and improves the total PF to 0.99. As can be seen in the spectrum of figure 4.24b, the main source current harmonic is of third order, which has already been reduced by 97%.

In principle the THD could be further improved by increasing the region where S_2 and S_3 switch but it has to be limited to around 15% of the maximum supply voltage when the capacitor voltage starts to present a very large ripple. Finally, similar results for a single-phase rectifier bridge with an inductive load are shown in figure 4.25. In this case, the current THD was reduced form 26% to 3.7%.

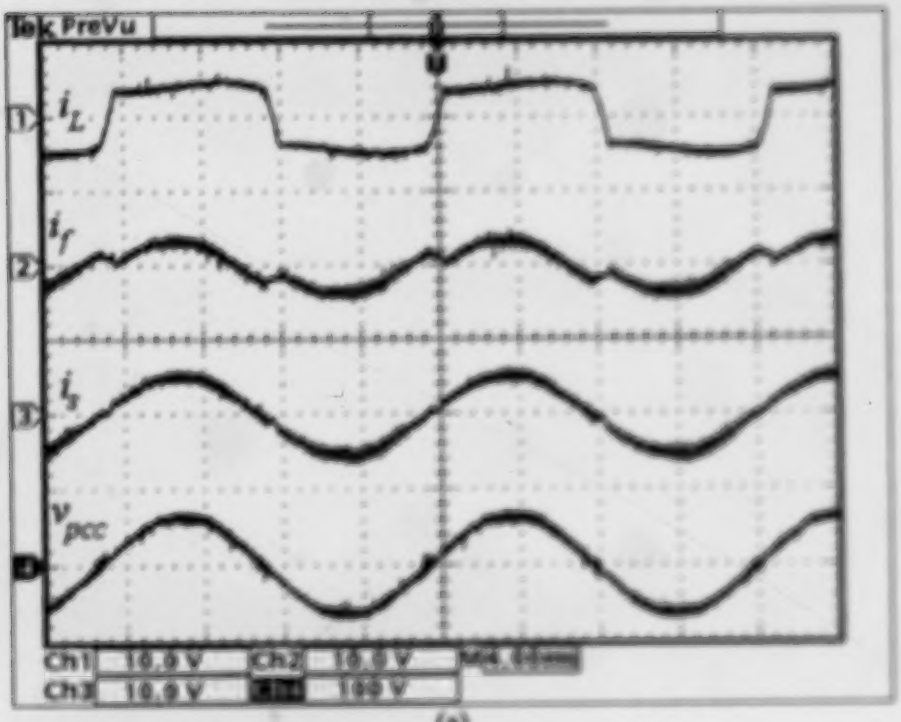


(a)

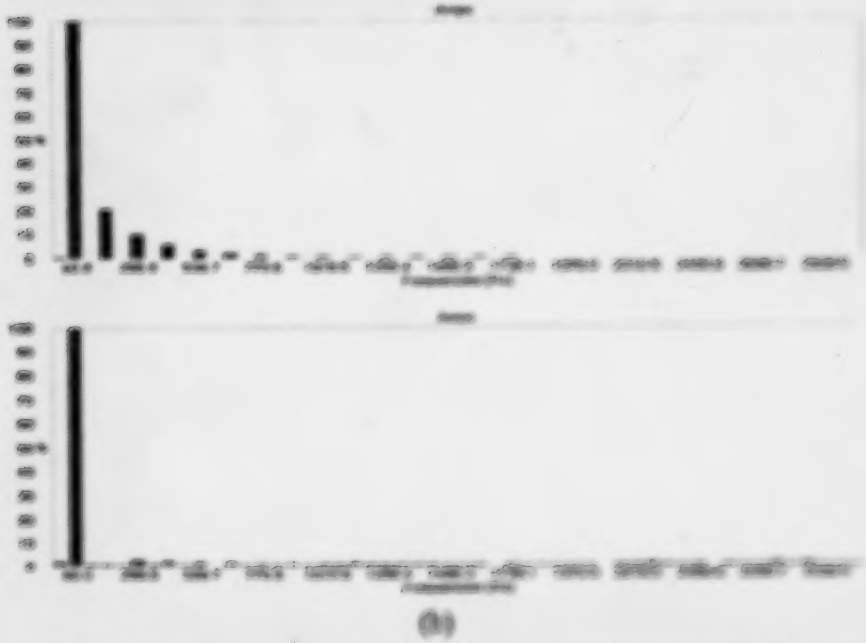


(b)

Figure 4.24 (a) Load current, power conditioner current, supply current and v_{pcc} with rectifier bridge with capacitive filter load with modified control strategy, (b) Harmonic spectrum for both load and supply current.



(a)



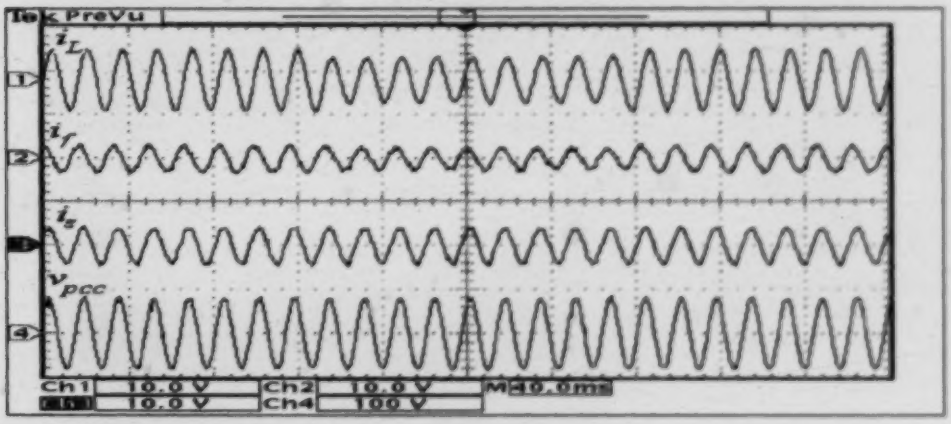
(b)

Figure 4.25 (a) Load current, power conditioner current, supply current and supply voltage with rectifier bridge with inductive load with the modified control strategy. (b) Harmonic spectrum for both load and supply current.

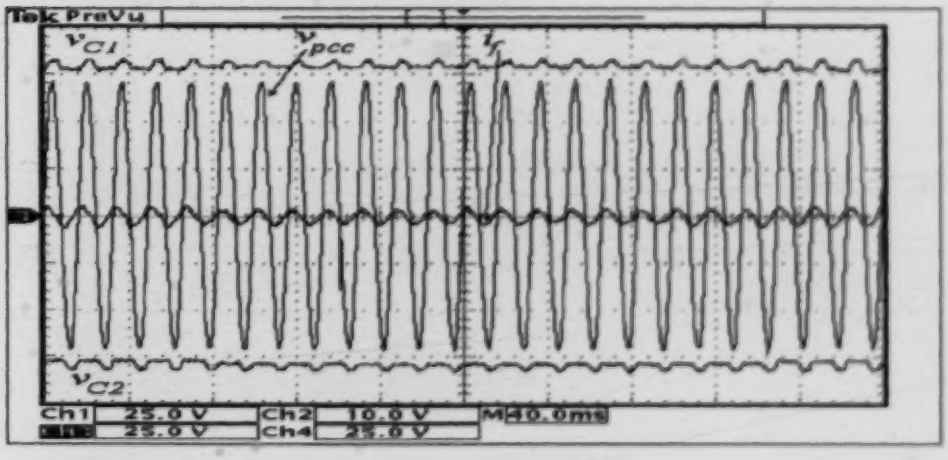
4.5.2.3 Transient analysis

Figures (4.26-4.29) document the performance of the SC scheme under four different transient analyses, which are: inductive load current variation, capacitive load current variation, source voltage variation and load power factor variation.

The waveforms in figure 4.26a,b shows the response of the switched capacitor based compensator when an inductive load current changes in a step-like manner from 1.0 p.u. to 0.7 p.u and back to 1.0 p.u. in a period of 0.4 s.



(a)



(b)

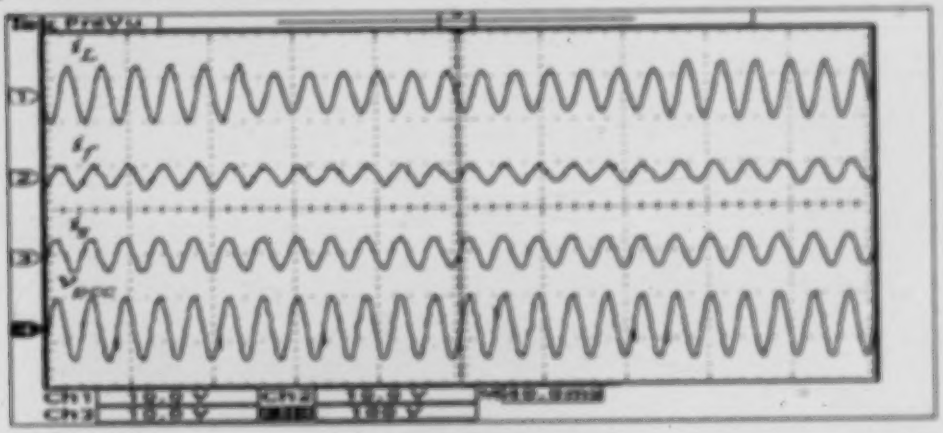
Figure 4.26 SC scheme performance for a cyclic inductive load current variation.

(a) i_L, i_f, i_s *and* v_{pcc}

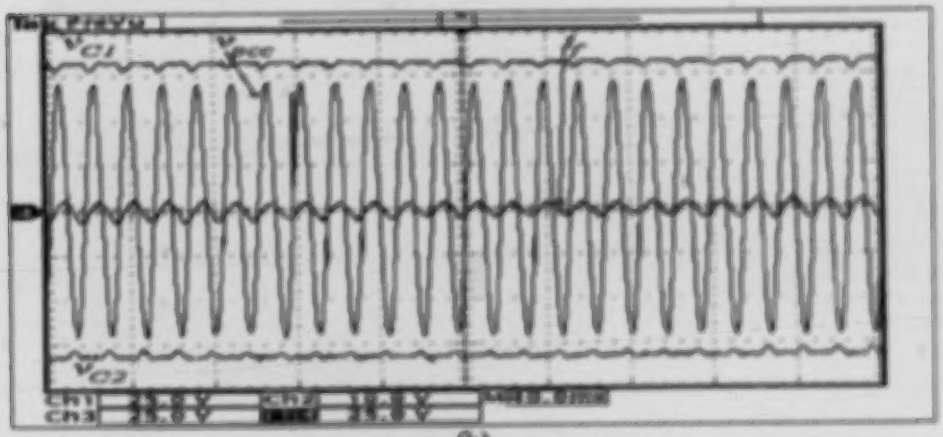
(b) v_{C1}, v_{C2}, v_{pcc} *and* i_f

There one can see that the proposed scheme is effective in tracking the required reference current with a fast dynamic response. Further, figure 4.26b reveals that the voltage ripple has some visible change, which is a factor of the current magnitude and capacitor size.

Similar results to the previous case are shown in figure 4.27a,b for a cyclic variation of a capacitive load current. Although the capacitor voltage tends to decrease from the initial capacitor voltage, the voltage control loop could keep it above the peak of the voltage at the point of common coupling that ensure proper operation of the SC scheme.



(a)



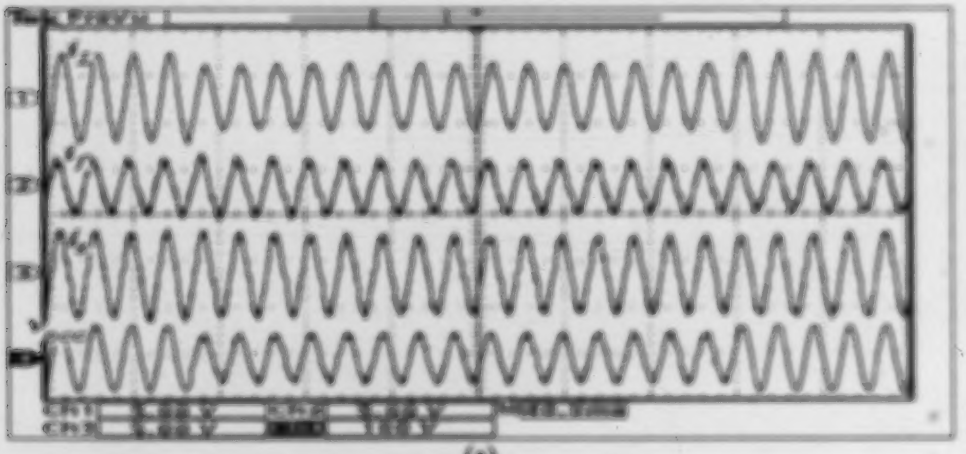
(b)

Figure 4.27 SC scheme performance for a cyclic capacitive load current variation.

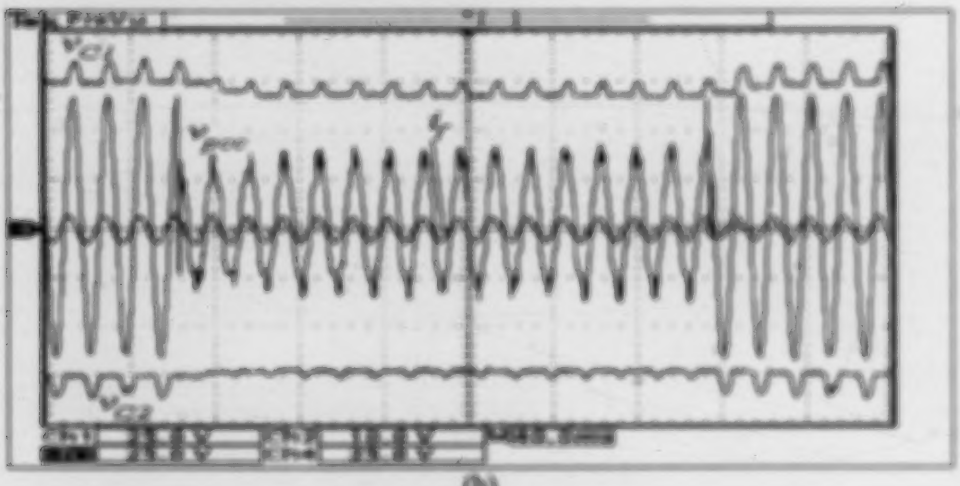
(a) i_L, i_s, i_f, and v_{pcc}.

(b) v_{C1}, v_{C2}, v_{pcc} and i_f.

Figure 4.28a,b shows the response of the SC scheme when the supply voltage changes in a step-like manner from 1.0 p.u. to 0.7 p.u and back to 1.0 p.u. in a period of 0.4 s when driving an inductive load. There one can see that the SC scheme could effectively deliver the required capacitive current during voltage sags to compensate for the reactive power in the system. One can further conclude from figure 4.28b that the voltage regulation loop could effectively maintain the capacitor voltages at a level that is higher than the supply voltage to allow the SC scheme to perform its function properly.



(a)



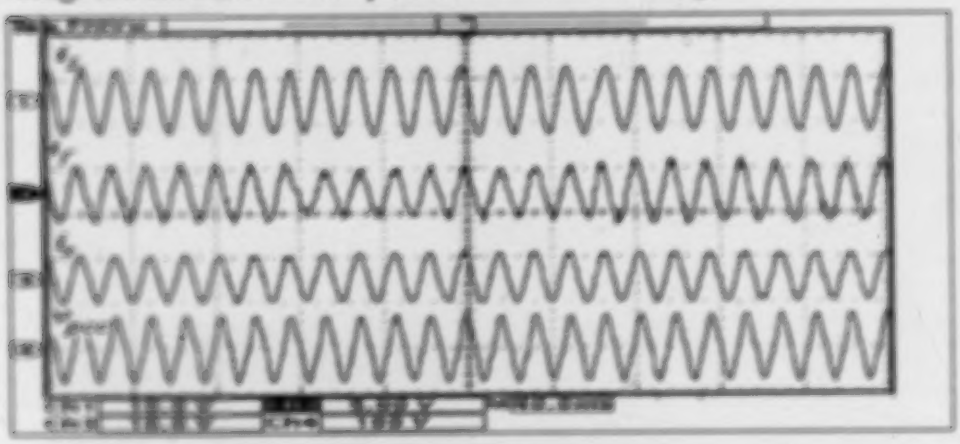
(b)

Figure 4.28 SC scheme performance for a cyclic supply voltage variation.

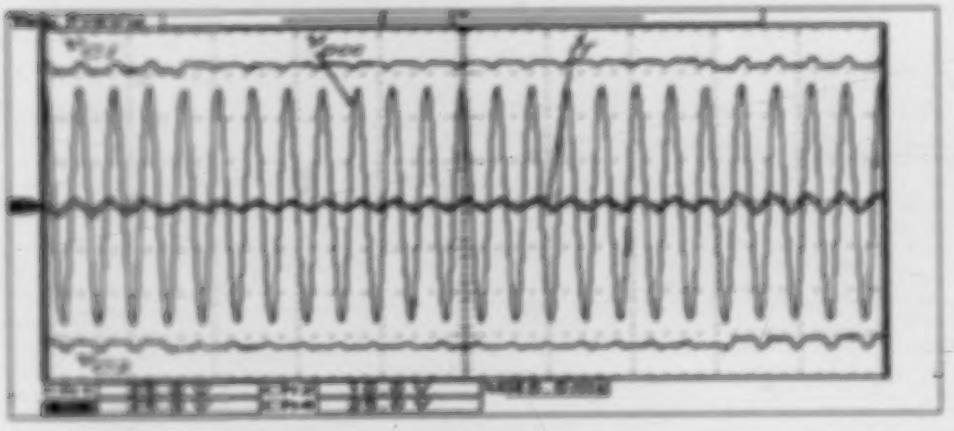
(a) i_1, i_2, i_3 *and* v_{pcc}.

(b) v_{C1}, v_{C2}, v_{pcc} *and* i_2.

Finally, the performance of the SC scheme to compensate for a sudden variation of the reactive power drawn by a linear load is shown in figure 4.29a,b. The load operates initially with a 0.87 lagging power factor that changes suddenly to 0.89 leading and then back to 0.87 lagging power factor in a period of 0.4 s. The figure also shows that the current injected in the ac mains by the power conditioner (i_f) yields almost total compensation of the reactive power drawn by the load, with an increase in the total power factor to almost 0.99. Further, the capacitor voltage loop is able to change the SC scheme capacitor voltage in a fast manner to compensate for this sudden change.



(a)



(b)

Figure 4.29 SC scheme performance for a sudden change in the load power factor.

(a) i_L, i_f, i_s and v_{pcc}.

(b) v_{C1}, v_{C2}, v_{pcc} and i_f.

4.6 Comparison between the Proposed SC Power Conditioner and Inverter-Based Power Conditioners

The objective of this section is to compare between the proposed SC scheme against the single phase inverter based powdr conditioner from the installation cost point of view. The economic comparison will be performed through a realistic numerical example. Assume that the test system that was used in the optimization procedure in Section 3.4.2.2 is the base for this comparison.

From there, and according to the available IGBT's in the market, one can see that a medium speed (600 V, 15 A) IGBT, IRG4pc30f, is suitable for the operation of the SC scheme. Further, a diode rectifier, GRpc2506A, should accompany each IGBT to form a bi-directional switch. For the inverter based power conditioner, a high speed (600 V, 12 A) IGBT, IRG4pc30ud, is suitable for the same application.

Table 4.1 summarizes the installation cost of both schemes, respectively. It states that there is a significant reduction in the total cost of the of the proposed SC scheme, ***$102.63***, which is almost 47% lower than the inverter based scheme, ***$191.18***, for the same kind of applications.

However, the installation cost may happen to be case dependent. Under different loading conditions, the SC scheme might be less or more economical than the inverter based power conditioner. Therefore, another system, which has higher voltage and power, is tested to investigate the effect of loading on the installation cost. Table 4.2 documents the new system parameters and the overall installation cost. The table reveals that the SC scheme installation cost, $2657, is 50% lower than its counterpart, the inverter based power quality conditioner, $5271, for the same loading conditions.

Finally, it can be concluded that the SC scheme is more economical than the inverter based power conditioner, and it has almost a constant trend of reducing the installation cost by approximately 50% for the same loading conditions.

Table 4.1 Comparison between the proposed SC power conditioner and inverter based power conditioners from the installation cost point of view for low power application

Comparison Criteria	*Inverter Based Power Conditioner*	*Proposed SC Power Conditioner*
System voltage	120 V	120 V
Rated current	5 A	5 A
Switching frequency	10-30 kHz	2-4 kHz
Number of active components	1-phase: 4 high speed (switches and diodes)	1-phase: 3 low speed bi-directional (IGBT+ bridge rectifier) switches
Cost of active components	IRG4pc30ud = $9.29 **Total cost (1)= 4*$9.29=$37.16**	IRG4pc30F = $4.12 Gbpc2506A = $3.91 **Total cost (1)= 3*8.03=$24.09**
Number of passive components	• 1x 3 mH inductor (5% of the inverter rating) • 1x Large DC capacitor (>4700μF)	• 1x 3 mH inductor (5% of the SC scheme rating) • 2 x small DC capacitors (~100-300 μF)
Cost of passive components	• Inductor (Hammond 195G10)= $57.3 • Capacitor (Panasonic EEG-AA2W362HLE) =$96.72 **Total cost (2)= $154.02**	• Inductor (Hammond 195G10)= $57.3 • 2 x Capacitor (Panasonic ECO-S2WB271DA) =2*$10.62=$20.24 **Total cost (2)= $78.54**
Total cost	**Total cost =(1)+(2) =$191.18**	**Total cost =(1)+(2) =$102.63**

Table 4.2 Comparison between the proposed SC power conditioner and inverter based power conditioners from the installation cost point of view for medium power application.

Comparison Criteria	*Inverter Based Power Conditioner*	*Proposed SC Power Conditioner*
System voltage	400 V	400 V
Rated current	250 A	250 A
Switching frequency	10-30 kHz	2-4 kHz
Number of active components	1-phase: 4 high speed (switches and diodes)	1-phase: 3 low speed bi-directional (IGBT+ bridge rectifier) switches
Cost of active components	Powerex CM400HA-24H = $260 **Total cost (1)= 4*$260=$1040**	Powerex CM400HU-24F = $185 Powerex R6201240XXX = $69 **Total cost (1)= 3*254=$762**
Number of passive components	• 1x 0.13 mH inductor (5% of the inverter rating) • 1x Large DC capacitor (~30,000 μF)	• 1x 0.13 mH inductor (5% of the SC scheme rating) • 2 x small DC capacitors (~3,000 μF)
Cost of passive components	• Inductor (3 parallel Hammond 195B150)= $1311 • 10 x Capacitor (3000 uF, 550V) =10*$292=$2920 **Total cost (2)= $4231**	• Inductor (3 parallel Hammond 195B150)= $1311 • 2 x Capacitor (3000 uF, 550V) =2*$292=$584 **Total cost (2)= $1895**
Total cost	**Total cost =(1)+(2) =$5271**	**Total cost =(1)+(2) =$2657**

4.7 Conclusions

A new control strategy that aims to mitigate some of the drawbacks for the proposed SC based power conditioner has been presented in this chapter. The main features of the new circuit are as follows:

- It provides an alternative switching scheme for hysteresis control that allows an increase in the current tracking capability of the scheme at the worst possible case for switched capacitor topologies: the zero crossing points of the ac line voltage.
- In addition, a voltage control loop is added to keep the capacitor voltages at certain required level that allows proper operation of the SC scheme with small capacitor sizes. Further, the energy balance concept in the energy storage capacitor is used to simplify the design of the voltage control circuit. The chapter has further presented some simulation results to evaluate the performance of the SC filter under steady state and transient operations to verify the effectiveness of the SC scheme and the design methodology used which proved that the scheme is capable of tracking different commands effectively under different conditions.
- For the compensator operating as an SVC independent of the load, it was shown that the it presents a fast speed of response for reference current variations and that it can keep close track of the reference current for sudden variations in the PCC voltage.
- Moreover, it was shown that the proposed switched capacitor converter could successfully compensate variations of linear and non-linear loads resulting in a source current with minor harmonic components and in phase with the fundamental voltage.
- Further, the experimental results confirmed that significant harmonic mitigation could be obtained with an average switching frequency as low as 3.0 kHz and has a fast speed of response as demonstrated by the transient analysis.
- Finally, from the installation cost point of view, it is proved that the proposed SC power conditioner could reduce the total cost by almost 50% when compared with the inverter-based scheme for the same kind of applications.

CHAPTER 5

Application Example: SC Based Harmonic Active Filter

5.1 Introduction

In the conventional passive filters, L-C is tuned to absorb harmonic currents generated by non-linear loads. But several drawbacks such as source-sink resonance, parameter variations, sensitivities to frequency variations, etc, reduce the effectiveness of the passive filter system. The current state of active filtering techniques requires high frequency PWM inverters to achieve the desired harmonic filtering and big energy storage to ensure constant dc voltage or current. For high power applications, the main aim of active filters is to eliminate or reduce the current harmonics. Because of economic considerations, reactive power compensation using active filters at the high voltage distribution level is not generally regarded as viable [4], because of the high voltage and its accompanying problems of isolation and series/parallel connections of

switches. Alternative approaches such as line-commutated thyristor converters are considered more suitable [42-43].

This chapter focuses on the application of the SC scheme in harmonic mitigation. Steady-state operation and transient analysis are carried out to analyze the performance of the scheme under different operating condition. Finally, experimental results are provided to demonstrate the validity of the analysis and design procedure.

5.2 Generation of the Reference Current for the Proposed Control Strategy

Two detection methods are chosen for generating the reference current for compensating harmonic currents for a given load. The first method is based on the extraction of harmonics using a 60 Hz band-stop filter [71], while the second detection method is based on the Adaptive Noise Canceling (ANC), which will be modified to generate the reference current that is required for the SC power conditioner to act as an active filter. Details of both techniques are given below.

5.2.1 Reference Current Generation Using Universal Active Filter (UAF)

A simple circuit that can be used to generate the harmonic reference current is shown in figure 5.1a. There one may see that the reference current, i_{ref} is obtained by using a 60 Hz band stop (reject) filter on the load current. In figure 5.1b, f_{notch} is the center frequency of the notch filter; f_1 and f_2 define the edges of the notch's stop band. However, careful design for the bandwidth of the filter and its performance to minor change in supply frequency should be counted. Therefore, a commercially available universal active filter chip (UAF42) that can be designed to get minimum phase and magnitude errors is used. Higher order filters can be implemented by cascading a number of these chips to get the required performance. The filter can be simply tested and adjusted using a square wave input as shown in figure 5.1c.

The complete control circuit for the SC active filter is shown in figure 5.2. There one can see that the reference current, i_{ref} is added to the regulating current,

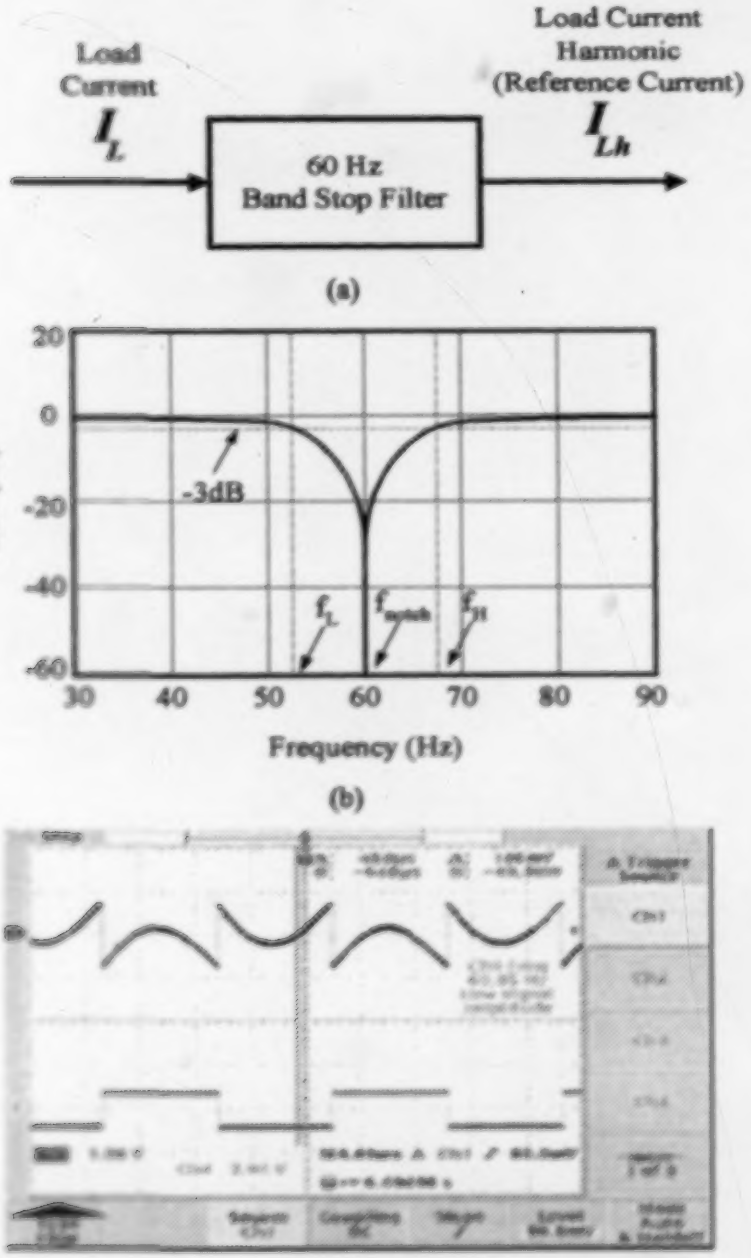


Figure 5.1 (a) Circuit for reference current generation. (b) General form of the notch filter response. (c) Output waveform from the universal active filter chip when it has a square wave input waveform

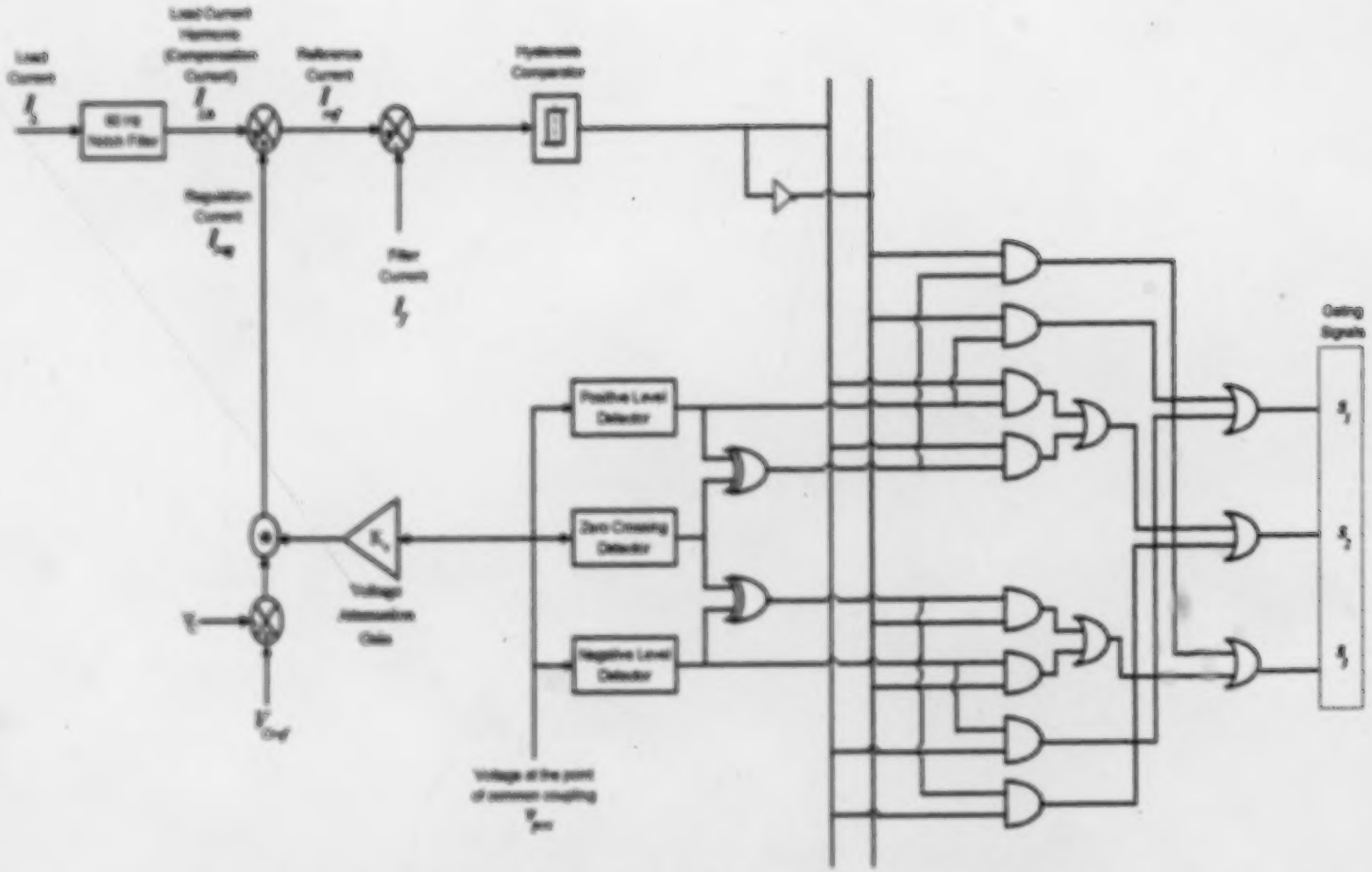


Figure 5.2 Complete control circuit for the SC system used in harmonic mitigation

i_{reg} to get the final current command i_c to the filter. Then, the command current is compared with the actual filter current, i_f, and the error is passed through a hysteresis window and a logic circuit that yields the desired gating signals for S_1, S_2 and S_3.

The simplicity of this technique, one chip, and fast response, offers many advantages for the operation of the filter over the other harmonic extraction techniques such as d-q reference frame, instantaneous reactive power theory, or negative sequence components extraction, as will be shown in the simulation results and experimental verification.

5.2.2 Reference Current Generation Using Adaptive Noise Canceling (ANC) Technique

In Chapter 3, Section 3.4.1.3, we discussed the application of the ANC technique for reactive power compensation. Further, it was concluded that by using an adaptive noise filter, we could get a signal that is equal to the active component of the load current, $i_{La}(t)$, that is subtracted from the load current, $i_L(t)$, to get the reactive component of the load current, $i_{Lr}(t)$, which is the reference current for the SC scheme.

In this section, however, we are looking for a reference current that only represents the harmonics currents, $i_{Lh}(t)$, in the system. Therefore, we are looking for a circuit that can generate a signal that is equal to both the fundamental active and reactive components of the load current that can be finally subtracted from the load current to get the harmonic current $i_{Lh}(t)$.

The circuit that generates the reference current of the proposed active filter is based on the scheme shown in figure 5.3. By modifying the ANC method, the fundamental component of the load current and voltage at the point of common coupling, $v_{pcc}(t)$, are mutually correlated. The voltage $v_{pcc}(t)$ is used as a reference for the circuit that is a continuously regulated closed loop system. Two adaptive filters process this reference input. One to produce an output which equals the active component of the load current signal $i_{La}(t)$ in amplitude and phase and the other to do the same function but for reactive component $i_{Lr}(t)$. The output of the adaptive

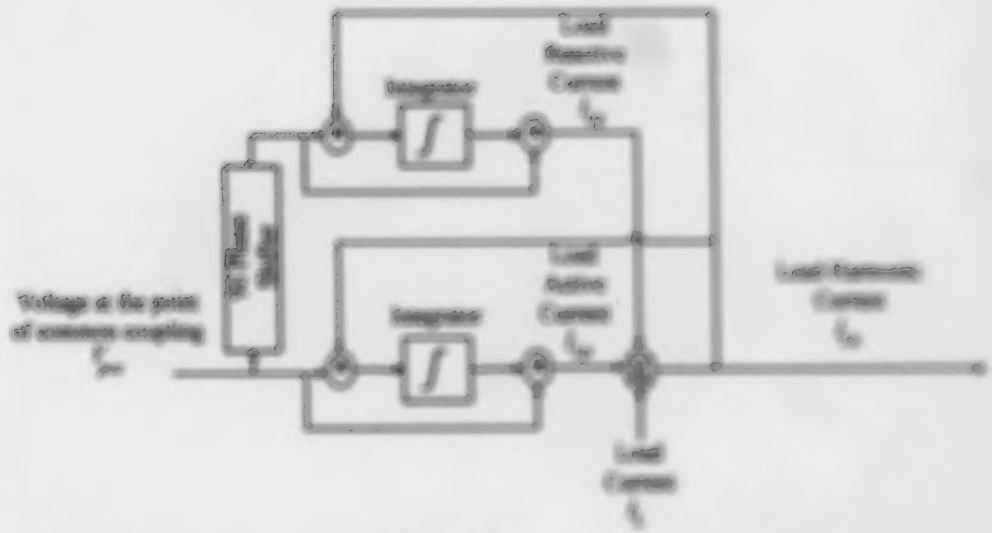


Figure 5.3 Scheme for generating the reference current of the power conditioner

filters is then subtracted from the actual load current $i_L(t)$ to obtain the harmonic component, $i_{Lh}(t)$. The system will reach its steady state when the integrators outputs are constant, which means that $i_L(t)$ is in phase with $v_{pcc}(t)$ and $i_{Lf}(t)$ has a 90° phase shift with respect to $v_{pcc}(t)$. Finally, i_{Lh} is added to the regulating current, i_{reg} to get the final current command i_c to the filter that is compared with the actual current of the SC filter, $i_f(t)$, and the error is passed through a hysteresis window and a logic circuit that yields the desired gating signals for S_1, S_2 and S_3.

5.3 Design Procedure

5.3.1 General Considerations

The capabilities of a power conditioner operating with hysteresis current control to quickly and closely track a current template depend on the possible values for di/dt and on the size of the hysteresis window (10). Fast and close tracking come at the expense of a high switching frequency and an alternative suitable to the application should be sought. According to (3.3) the inductor size affects the value of di/dt for modes 1 and 2 while the capacitor size, which influences the relative

magnitude of the capacitor voltage with respect to the PCC voltage, affects the value of di/dt for mode 2. Small inductors increase the values of di/dt enhancing the capabilities of the power conditioner to filter high order harmonics. On the other hand small capacitors reduce the stiffness of the capacitor voltage waveform, resulting in bigger variations for a given variation of the current template. This can result in either high peak voltages that yield higher voltage ratings for the power switches or low valley voltages that violate the need for the capacitor voltage to be always higher than the PCC voltage.

In conclusion, the choice of the passive elements L-C is rather complicated which prompted the use of a systematic optimization procedure that may allow the choice of the system components for different applications.

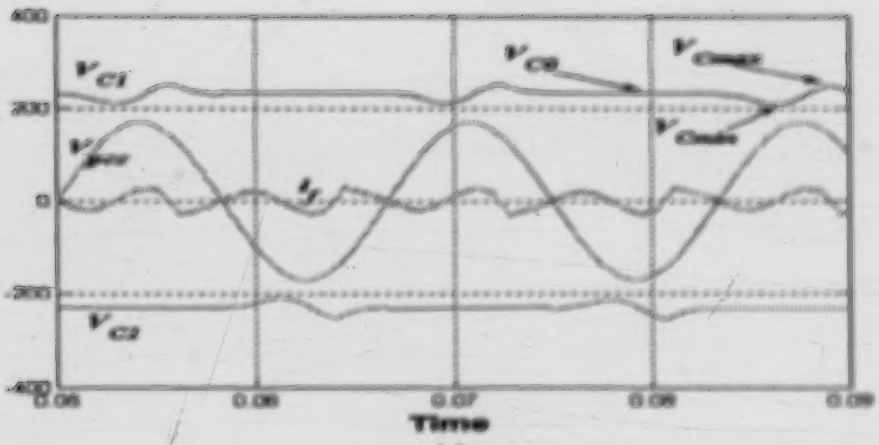
5.3.2 Calculating Circuit Components

The design procedure described in Section 3.4.2.3 is adopted to determine the SC components when a non-linear load current waveform of 58% total harmonic distortion is under consideration and for a given hysteresis window, ΔI, of 5%. The results, such as those presented in figure 5.4a,b are then used to evaluate the performance of the filter in terms of the THD of the source current (i_s) and average switching frequency. Then the values of L_f and C_f are changed according to the algorithm of the flow chart of figure 3.12 and the simulation process is repeated.

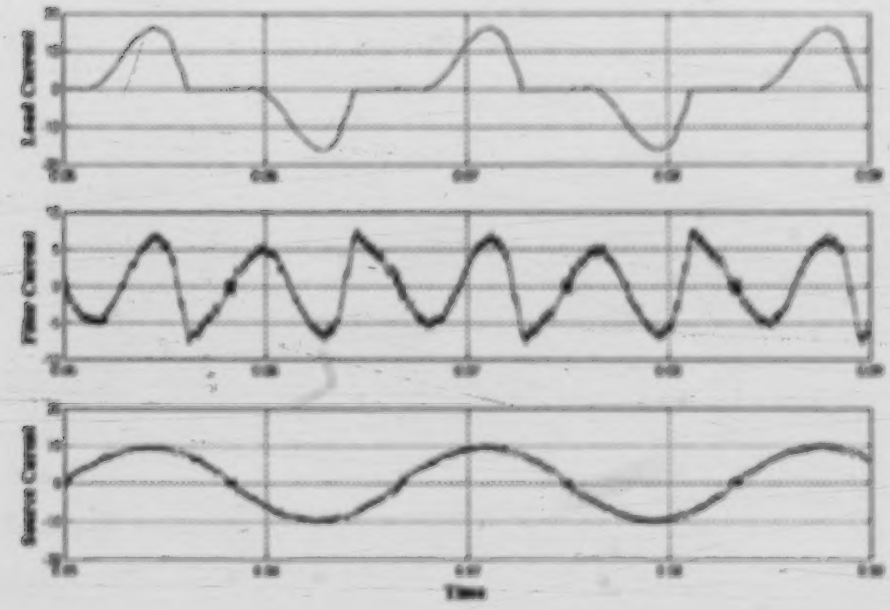
By selecting the initial capacitor voltage at certain level V_{C0}, that will be the reference voltage for the capacitors voltage regulation loop, and selecting V_{Cmin} to be at a certain minimum level bigger than the peak of v_{pcc}, the capacitor value can be calculated. Then, the optimization technique is performed to provide a set of graphs as shown in figure 5.5, which allow the choice of optimum values for L_f & C_f.

One can see from figure 5.5 that the maximum average switching frequency lies between 2.0 and 7.0 kHz, which insures that the switching losses are small and the system doesn't need big cooling requirements.

By investigating the figures, for a supply voltage of 120 V, an inductor L_f = 4.0 mH and a capacitor C_f = 230 uF will result in THD of 3.8% and switching frequency of 3.7 kHz, with V_{Cmax} of 250V, and V_{Cmin} of 225V and V_{C0} of 235V.



(a)



(b)

Figure 5.4 Typical waveforms for: (a) v_{pcc} and capacitor voltages, v_{c1} & v_{c2} (b) Load current i_L, filter current i_f and source current i_s.

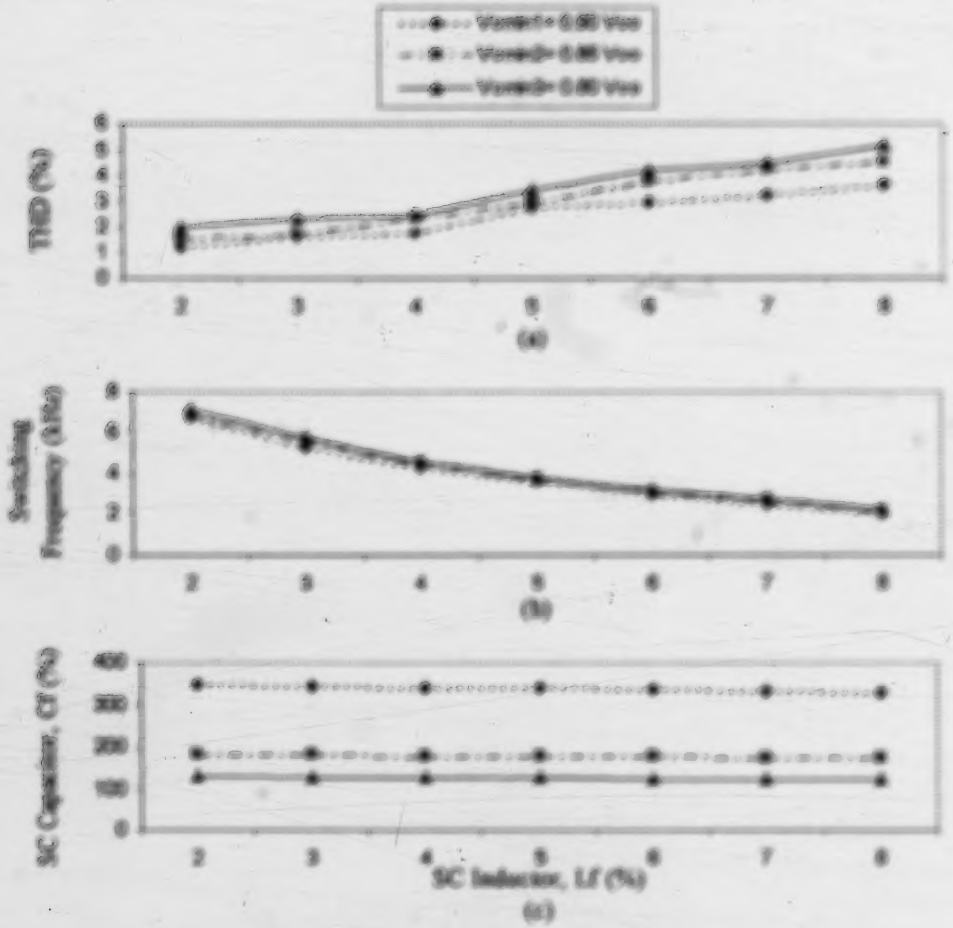


Figure 5.5 Optimization procedure results

5.4 Simulation Results

The simulation is performed with the PSCAD software program using both the UAF and ANC techniques to have a complete overview of the performance of the SC scheme under different reference generation circuits that may assist the choice of a particular one.

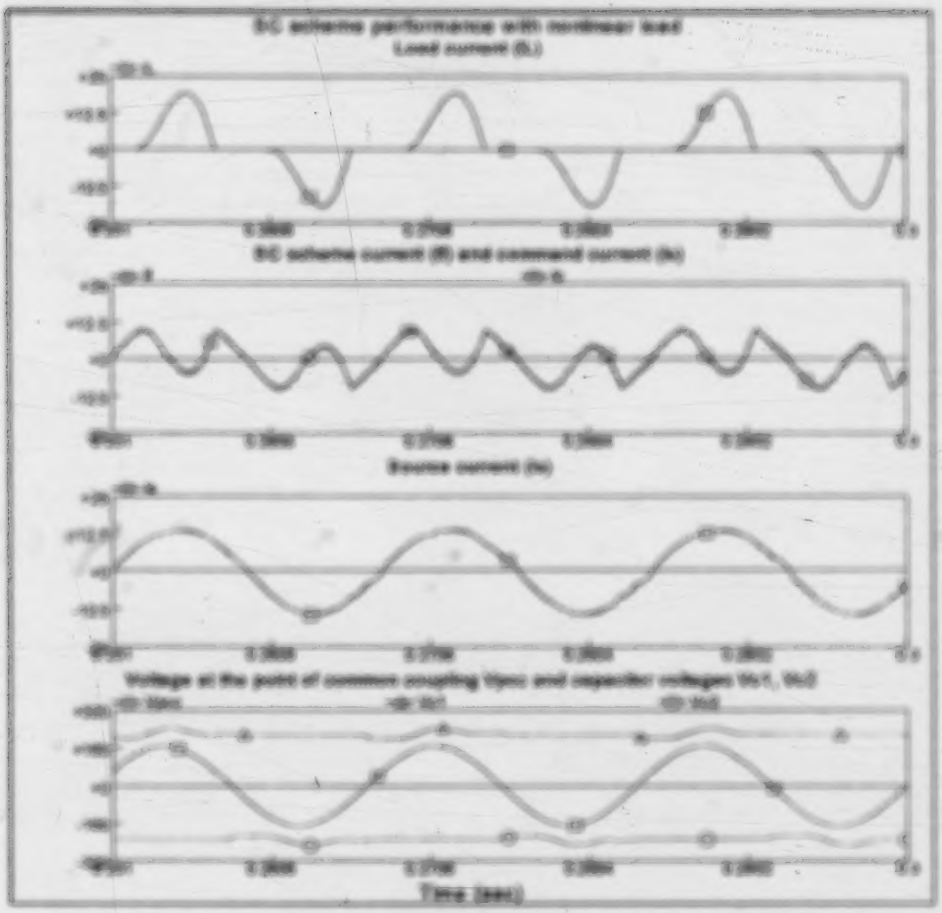
The system parameters used in the simulation are as follows:

- Utility System: A regulated single-phase ac supply of 120 Vrms, 60 Hz; Line resistance, $R_s = 0.1\ \Omega$, Line inductance, $L_s = 0.1$ mH
- Switched Capacitor Filter: $C_f = 230\ \mu F$, $L_f = 4.0$ mH,
- Critical Load: A 5.0 % reactor is used in the ac side a non-linear load. The non-linear load is modeled as follows:
  - A diode rectifier bridge consisting of the following values: (R_L = 22.0 Ω, $C_{dc} = 940\ \mu F$) and ($R_L = 5.0\ \Omega$, $L_L = 50$ mH).
  - A thyristor rectifier bridge consisting of the following values: R_L = 5.0 Ω, $L_L = 50$ mH, and firing angle δ=30°.

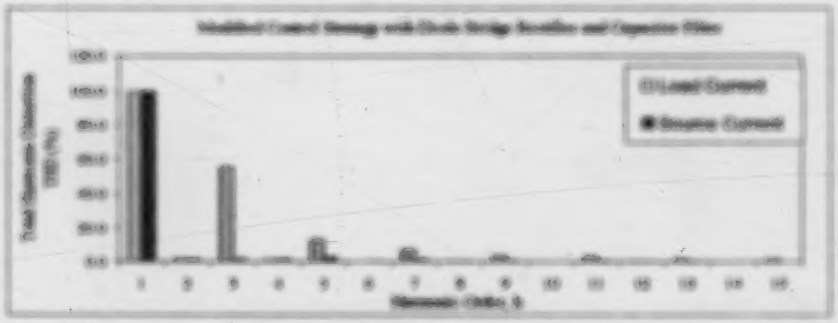
This section is organized as follows: Section 5.4.1 presents the simulation results in steady state when the SC scheme is using the UAF technique for reference current generation. Section 5.4.2 presents the simulation results in steady state when the SC scheme is using the ANC technique for reference current generation. Section 5.4.3 gives a comparison between the results of the two reference current generation schemes. Finally, Section 5.4.4 presents a number of tests to evaluate the performance of the compensator under different transient conditions, such as variation in the bus voltage and load current.

5.4.1 Simulation Results with Reference Current Generation Using UAF Technique

The simulation results for different cases are shown in Figures (5.6-5.8). Further, the numerical values for THD resulting from the odd harmonics from 3rd to the 15th


DC scheme performance with nonlinear load
Load current (iL)
DC scheme current (if) and command current (ic)
Source current (is)
Time (sec)

(a)



(b)

Figure 5.6 (a) Simulation waveforms with UAF technique for a single-phase diode bridge rectifier circuit with capacitor filter: load current i_L , filter current i_f , source current i_s , and v_{pcc}, v_{c1} & v_{c2}

(b) Harmonic spectrum for the load and source currents.

in the load and source currents along with the corresponding switching frequency for each case is tabulated in Table 5.1.

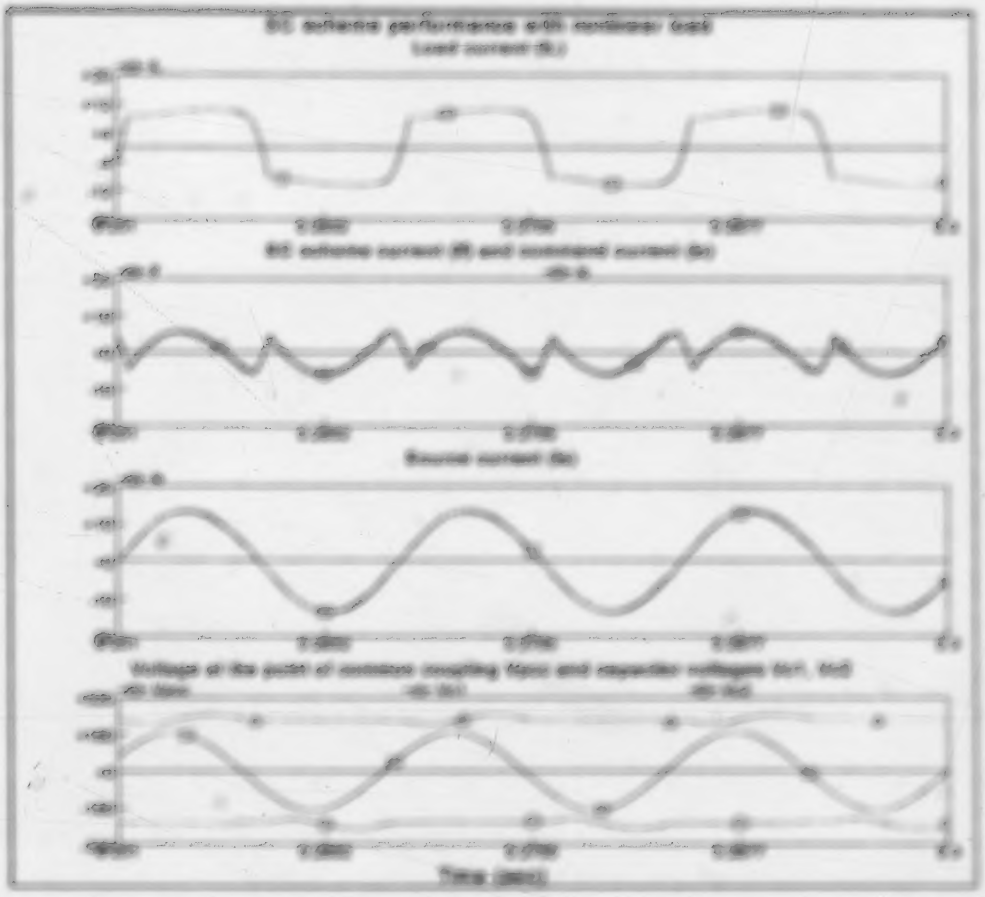
The following variables are displayed:

- The load current i_L, for different loads and its harmonic spectrum.
- The command current to the SC scheme, i_c, and the SC output current, i_f, in one figure to show how close the SC current can track any command current and to investigate the effect of the standrad and modified control strategies on this current.
- The source current i_s, for different loads and its harmonic spectrum.
- Finally, the voltage at the point of common coupling v_{pcc}, and capacitor voltages, v_{c1} & v_{c2}, that shows how the SC scheme satisfy the requirements for the SC scheme to operate properly.

The Load and source currents waveforms in Fig 5.6a reveals that the filter is effective in compensating for load harmonic current when using the modified control strategies. Further, the spectrum shown in Fig 5.6b verify these results by showing the improvement of individual harmonic components in both cases. It is worth mentioning that the SC scheme could achieve its performance with a switching frequency that ranges from 3.1 to 4.2 kHz depending on the type of the load used in the simulation.

Other simulaions results is carried out to evaluate the performance of the SC filter for different other loads as shown in figure 5.7 to figure 5.8. Table 5.1 documents the above results and states that the total harmonic distortion of the source current when using the UAF technique with the modified control strategy is as follows:

- For the diode bridge rectifier with capacitor filter the THD is reduced from 58.0% to about 4.1% (92.4% reduction).
- For the diode bridge rectifier with inductive load the THD is reduced from 32.0% to about 2.4% (92.5% reduction).
- For the thyristor bridge rectifier with inductive load the THD is reduced from 32.0% to about 2.7% (91.5% reduction).

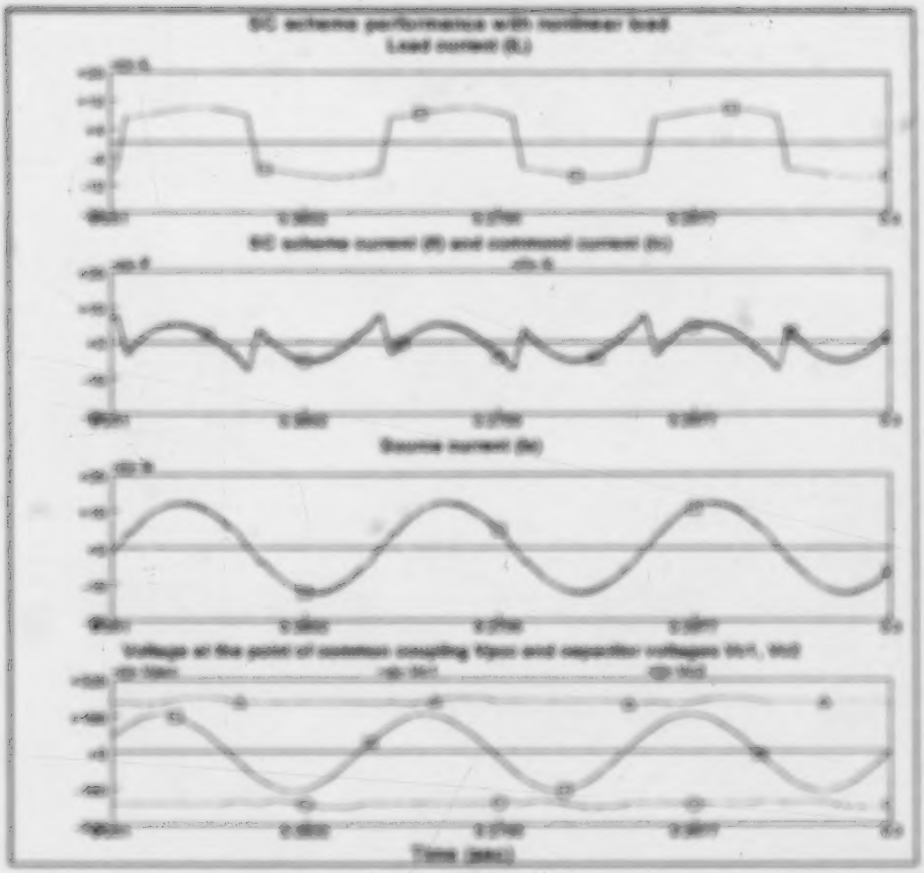


(a)

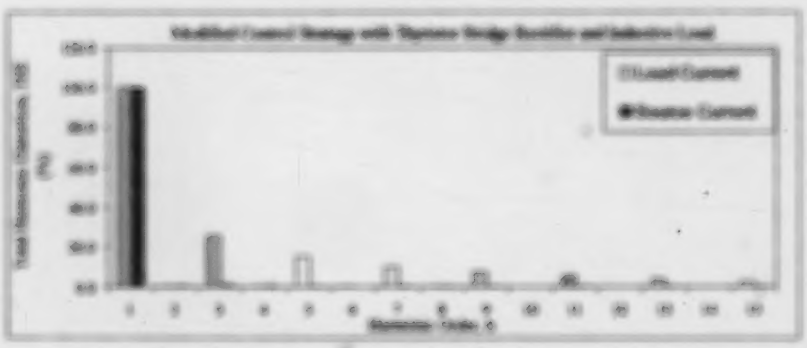
(b)

Figure 1.7 (a) Simulation waveforms with UAF technique for a single-phase diode bridge rectifier circuit with inductive load: load current i_L, filter current i_f, source current i_s, and v_{gate}, v_{cf} & v_{cl}

(b) Harmonic spectrum for the load and source currents


SC scheme performance with nonlinear load
Load current (iL)
SC scheme current (if) and command current (ic)
Source current (is)
Voltage at the point of common coupling Vpcc and capacitor voltages Vc1, Vc2
Time (sec)

(a)



(b)

Figure 5.9 (a) Simulation waveforms with UAF technique for a single-phase thyristor bridge rectifier circuit with inductive load: load current i_L, filter current i_f, source current i_s, and v_{pcc}, v_{c1} & v_{c2}

(b) Harmonic spectrum for the load and source currents

Table 5.1 Load current THD, source current THD, and switching frequency (F_s), for different types of simulation when using both UAF reference generation technique.

	Reference Current Generation Using UAF Technique		
	Diode bridge		**Thyristor bridge**
	Capacitor filter	**Inductive load**	**Inductive load**
Load Current THD (%)	38.0	32.0	32.0
Source Current THD (%)	4.1	2.4	2.7
F_s (kHz)	3.5	4.2	4.0

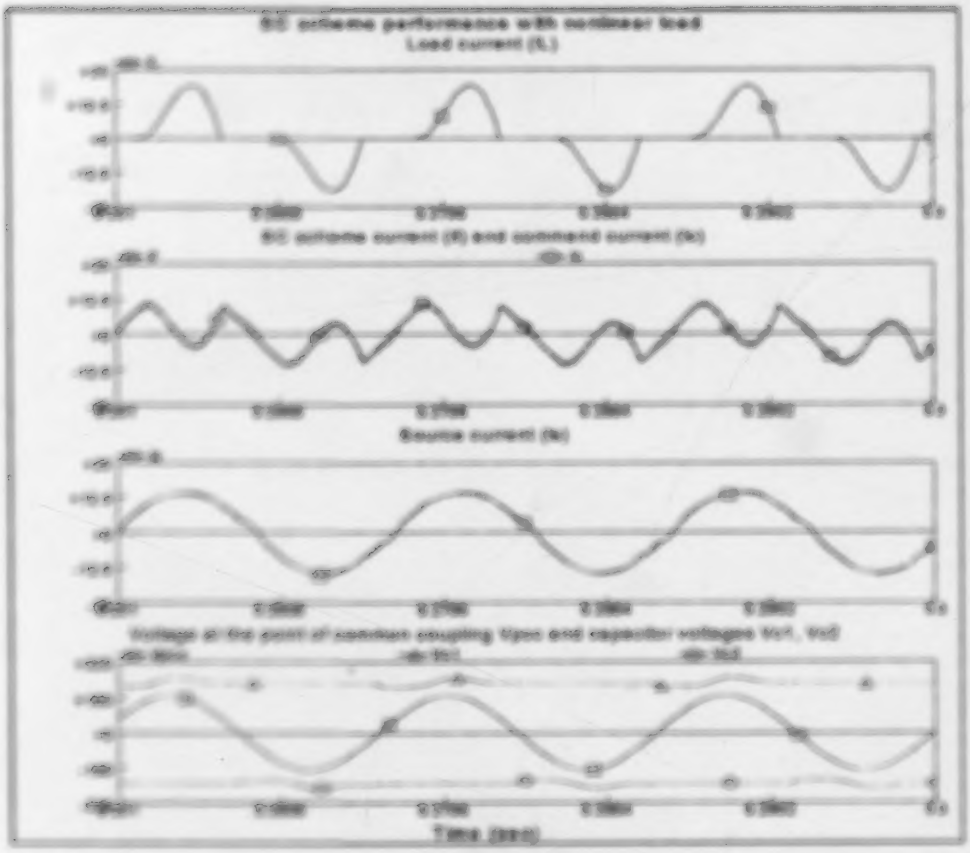
5.4.2 Simulation Results with Reference Current Generation Using ANC Technique

The simulation results for different cases are shown in figures (5.9-5.11). Further, the numerical values for THD resulting from the odd harmonics from 3rd to the 15th in the load and source currents along with the corresponding switching frequency for each case is tabulated in Table 5.2.

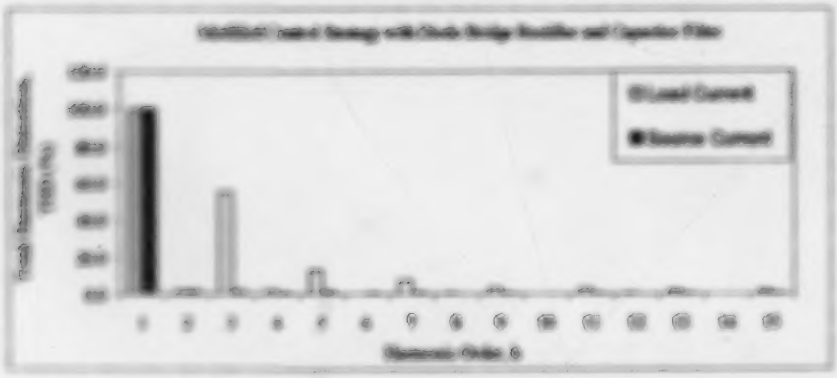
According to Table 5.2, the THD of the source current reveals that the filter is effective in compensating for load harmonic current and reducing the total harmonic distortion of the source current when using the ANC technique with the modified control strategy as follows:

- For the diode bridge rectifier with capacitor filter the THD is reduced from 38.0% to about 3.7% (93.6% reduction).
- For the diode bridge rectifier with inductive load the THD is reduced from 32.0% to about 2.1% (93.5% reduction).
- For the thyristor bridge rectifier with inductive load the THD is reduced from 32.0% to about 2.64% (91.7% reduction).

Finally, the SC scheme could achieve its performance with a switching frequency that ranges from 3.24 to 4.4 kHz.



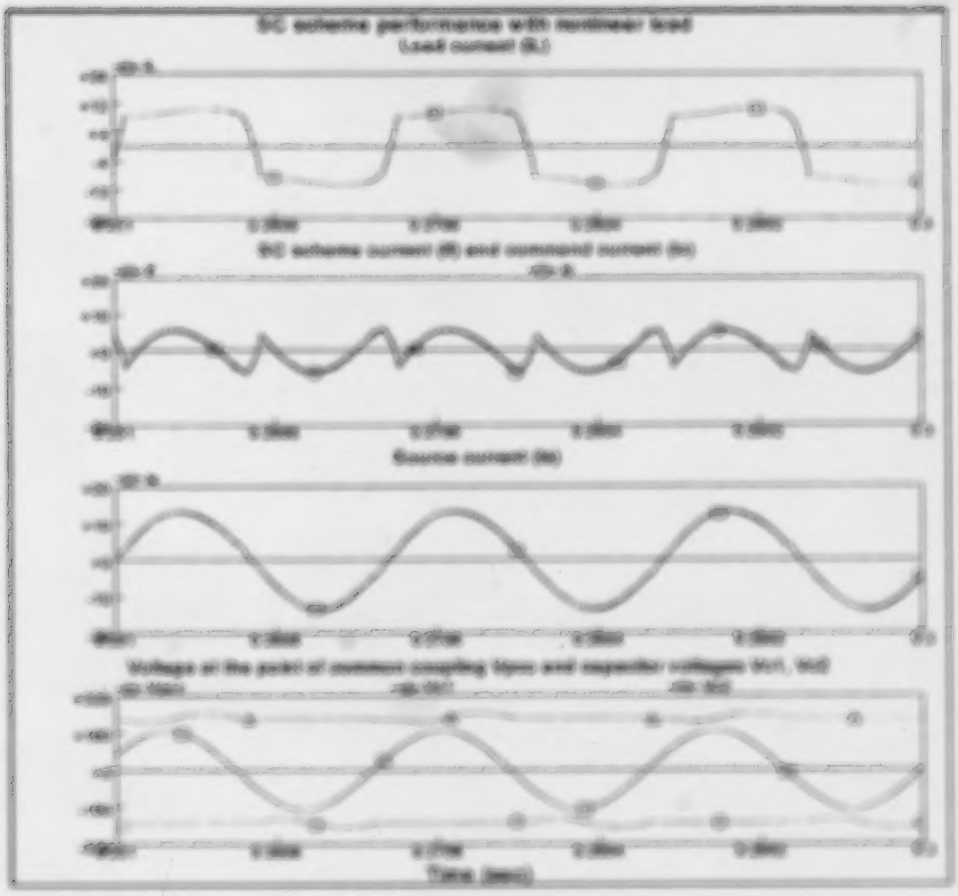
(a)



(b)

Figure 7.9 (a) Simulation waveforms with ANC technique for a single-phase diode bridge rectifier circuit with capacitor filter: load current i_L, filter current i_f, source current i_s, and v_{pcc}, v_{LC} & v_{DC}

(b) Harmonic spectrum for the load and source currents

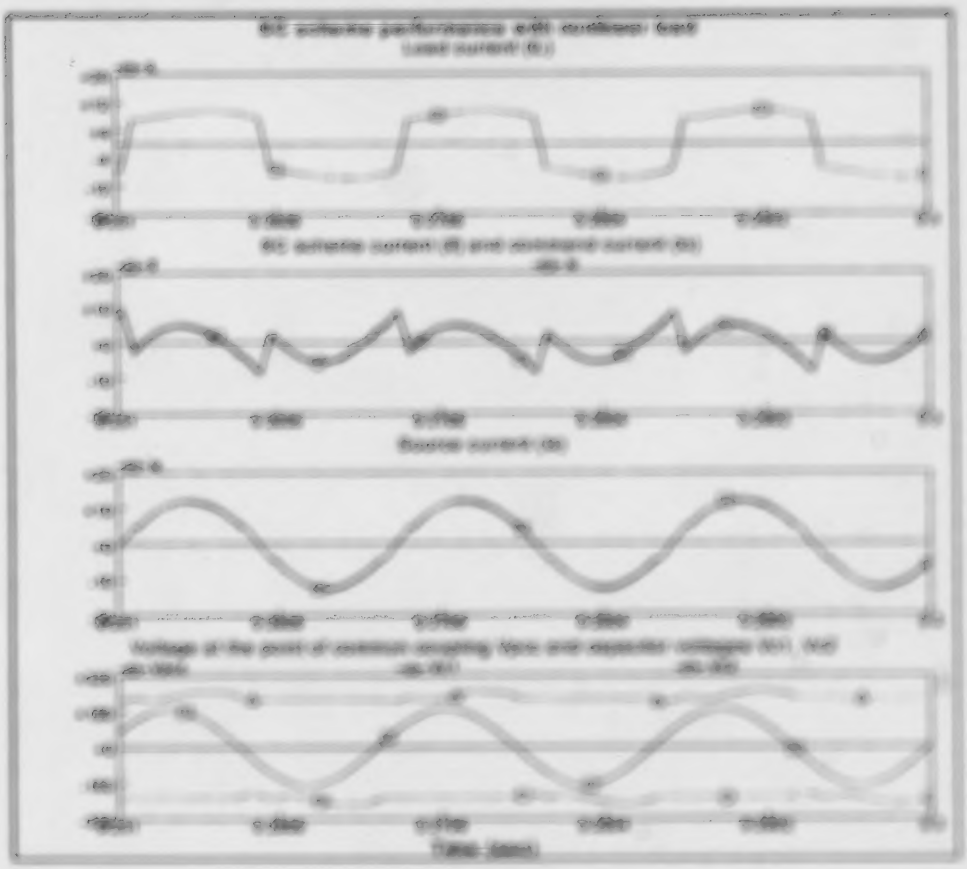


(a)

(b)

Figure 5.10 (a) Simulation waveforms with ANC technique for a single-phase diode bridge rectifier circuit with inductive load: load current i_L, filter current i_f, source current i_s, and η_{pwr}, η_D & η_{ID}

(b) Harmonic spectrum for the load and source currents



(a)

(b)

Figure 7.11 (a) Simulation waveforms with ESC for a single-phase thyristor bridge rectifier circuit with inductive load: load current i_o, filter current i_f, source current i_s, and v_{pcc}, v_o, & v_{ab}

(b) Harmonic spectrum for the load and source currents

Table 4.2: Load current (THD), source current (THD) and switching frequency (F_s) for different types of simulation when using both ANC reference generation techniques

	Reference Current Generation Using ANC Technique		
	Diode bridge		Thyristor bridge
	Capacitive filter	Inductive load	Inductive load
Load Current THD (%)	48	30	30
Source Current THD (%)	3.7	3.1	3.09
θ_1 (deg)	0.0	0.0	0.0

5.4.3 Comparison Between the Performance of the SC Scheme under the Two Reference Generation Circuits

Table 5.3 documents the basic differences between the two reference generation schemes in terms of the number of components, cost, magnitude and phase errors, control complexity, switching frequency, THD, and easiness of implementation. The comparison is done based on the theory of operation of both schemes and the results obtained from the simulation results.

Table 5.3 Comparison between the performance of the SC scheme under UAF and ANC reference generation schemes.

Comparison criteria	*UAF technique*	*ANC technique*
Number of components	One commercial chip	Four multipliers, two integrators, phase shifter, and summer.
Cost of components	Low	High due to the greater number of components. Further, the multipliers are especially expensive.
Magnitude and phase errors	Have minor magnitude and phase errors.	Self-adjustable to eliminate any magnitude or phase errors.
Control complexity	Easy to adjust especially the chip has software, which can model it for different types of filters and different orders.	Difficult to adjust due to the minor difference in the time constants of the integrators and the adjustment of the multipliers.
Switching frequency	3-4.2 kHz	3-4.5 kHz
THD	<5%	<5%
Implementation	Easy	Hard

The table reveals that both the schemes are effective in generation of the reference current that enables the SC scheme to inject the required compensation current to decouple the load harmonics current from the supply. Further, both the reference generation circuits could achieve their function with a small switching frequency. However, the UAF circuit is easy to implement, cost effective, and easy to adjust which makes it more suitable for our application.

5.4.4 Transient Analysis

This section discusses the performance of the SC compensator under transient conditions. Simulation results are presented to demonstrate the speed of response of the proposed compensator.

5.4.4.1 Cyclic variations in the load current

Figure 5.12 shows the response of the SC based active filter when the load changes in a step-like manner from 1.0 p.u. to 2.0 p.u and back to 1.0 p.u. in a period of 0.33 s.

When the supply voltage is applied, the output of the control circuit has not yet provided the steady state value of the reference current. Hence the harmonic component of the load current is supplied by both the supply and the SC filter. Moreover, the SC capacitors will be charged up to a bigger value than the supply voltage due to the inrush current of the transient. However, in the second cycle, the system will reach its steady state and the utility will supplement the energy in the capacitor to keep its voltage to prescribed value. Except for the first cycle, the control circuit has almost no other time delay. Therefore the transient response will be good.

At the tenth cycle, when the circuit is subjected to an increase in the load current, the utility source current responds immediately and stabilizes at the new value. Further, one can see the capacitor voltage will drop owing to the release of stored energy due to the increase in the current. However, it always maintains a sinusoidal source current. This drop in the capacitor voltages is compensated

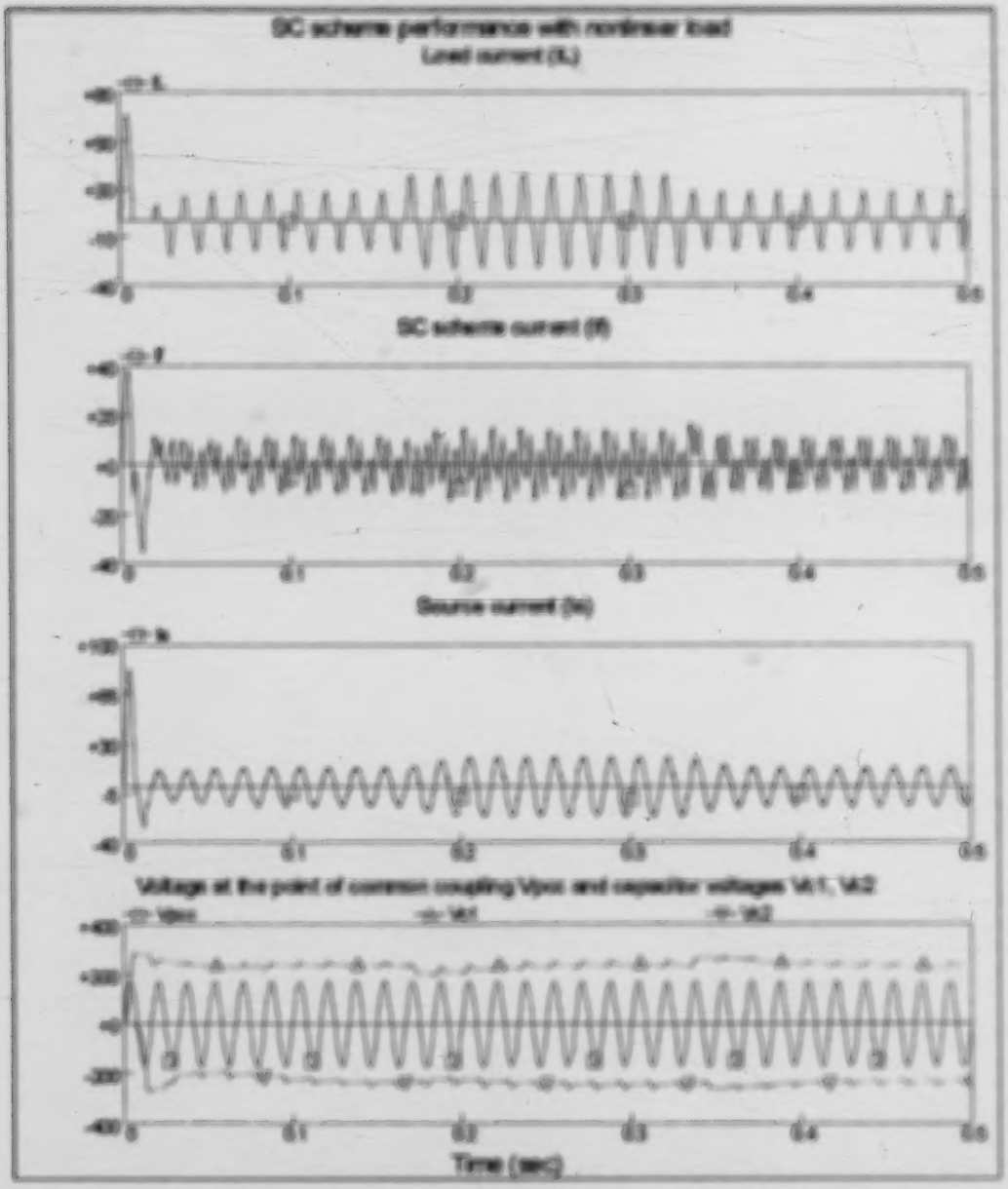


Figure 5.12 Simulation results for transient response of the SC filter for a step increase and decrease in the *load current* at the tenth cycle and twentieth cycle respectively

a- Load current,

b- Filter Current,

c- Source current,

d- v_{pcc}, v_{c1} & v_{c2}

by the utility in the next few cycles to keep the capacitor voltages at the required level.

At the twenties cycle, a step decrease of the peak load current by 50% is applied. From the simulation, although there is an increase in the capacitor voltage at the transition point, the current injected in the ac mains by the SC filter (i_s) follows closely the command current (i_c) and that yields almost total compensation of the harmonic current drawn by the load. However, if the capacitor voltage should be limited without exceeding a certain boundary, additional circuit should be added to let the utility current change immediately after the voltage limit is encountered. The circuit should estimate the extra fundamental utility current needed by the SC scheme to return the capacitor voltage to its present value before the beginning of the next cycle.

As a conclusion for the behavior of the SC based active filter for a cyclic change in the load current, the filter is effective in tracking the required reference current with a fast dynamic response. The voltage regulation loop is effective in charging or discharging the filter capacitors in a fast manner to keep the capacitor voltages at the specified limits. In the period of steady state operations, the initial capacitor voltage, V_{C0} is found to be (230V), the maximum capacitor voltage, $V_{C_{max}}$ is (252V) and the minimum capacitor voltage, $V_{C_{min}}$ is (218V). However, it is worth mentioning that the minimum capacitor voltages is close to the peak supply voltage for certain loads, and careful design procedure for the scheme elements should be done to avoid any system instability. Finally, the maximum capacitor voltage can be limited to avoid switches or elements failure.

5.4.4.2 Cyclic variations in the supply voltage

In this test, the response of the SC filter for a cyclic variation in the supply voltage is presented. As done in the previous section, the supply voltage changes in a step-like manner from 1.0 p.u. to 0.75 p.u and back to 1.0 p.u. in a period of 0.33 s.

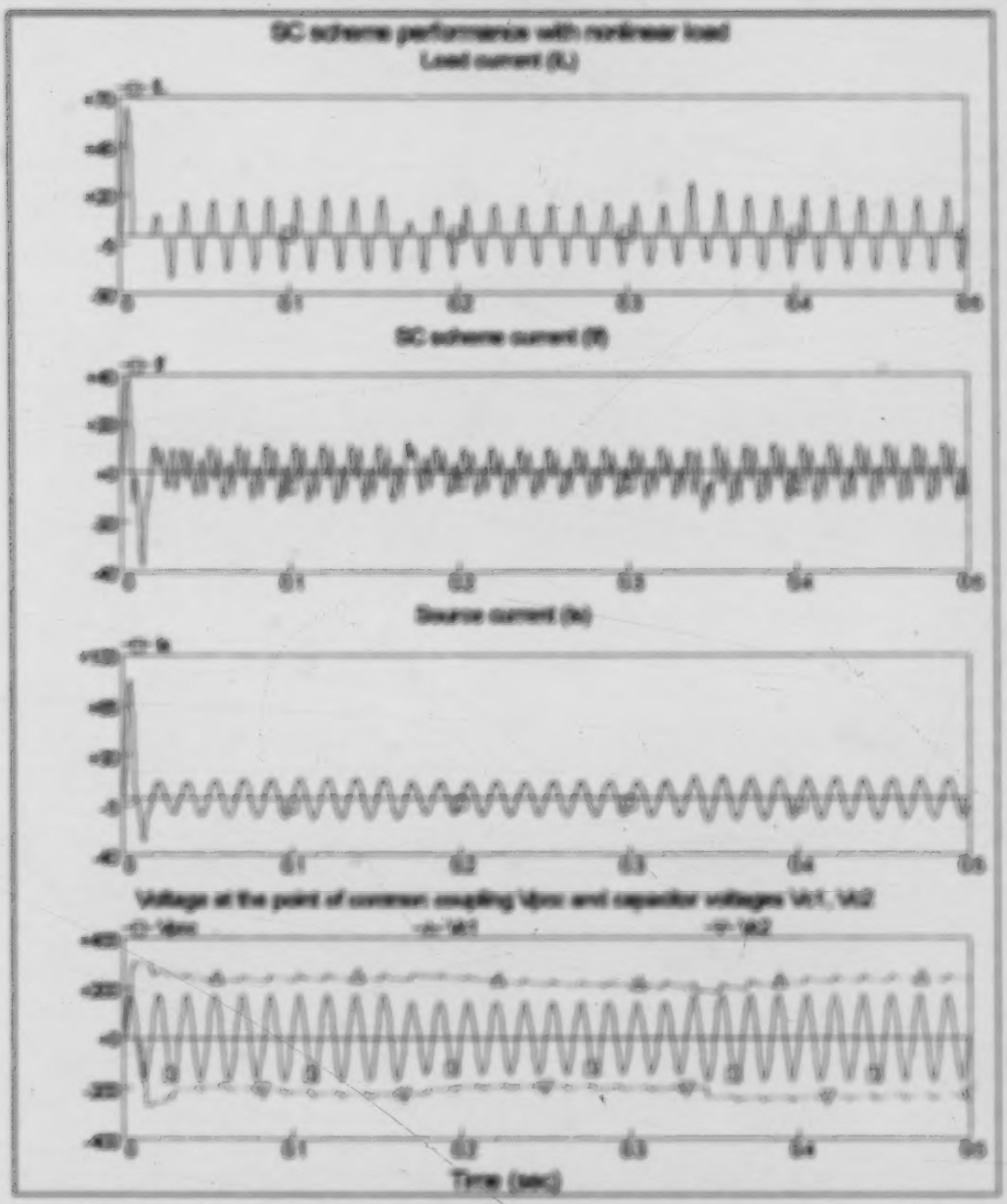


Figure 5.13 Simulation results for transient response of the SC filter for a step increase and decrease in the v_{pcc} at the tenth cycle and twentieth cycle respectively.

a- Load current,

b- Filter Current,

c- Source current,

d- v_{pcc}, v_{c1} & v_{c2}

In the test, it is assumed that the load under consideration has no voltage stabilizer in the front end. Therefore the load current will feel any changes in the supply voltage and responds correspondingly.

For the first ten cycles, the SC scheme goes through the start up process described in the previous section, and then the capacitor voltage stabilizes at the specified value. However, at the tenth cycle when there is a sudden sag in the supply voltage, the capacitor voltage starts to decrease and stabilizes at a value below the reference one. This happens due to the fixed proportional controller, K_{cp}, in the capacitor voltage loop. As a matter of fact, in this case, this gain should be increased to provide more active current to supplement the loss of capacitor energy to keep the capacitor voltage at the reference value. However, one can see from the simulation, that the filter could still provide a current, which maintains a sinusoidal supply current. Thanks to the voltage regulation loop, the capacitor voltage changes proportionally to the supply voltage. Therefore, the capacitor voltage in this situation will always remain higher than the supply voltage, which allow the SC scheme to perform it operation properly and in a fast manner as seen in figure 5.13. This can further be confirmed at the twentieth cycle when the supply voltage return to its original value. The capacitor voltage could respond immediately to cope for the supply voltage changes, and to maintain a sinusoidal ac main current.

5.4.4.3 Supply voltage variation with a constant load current

In this test, the response of the SC filter for a cyclic variation in the supply voltage while the load current is maintained constant during the whole operation is presented, as shown in figure 5.14. As done in the previous section, the supply voltage changes in a step-like manner from 1.0 p.u. to 0.75 p.u and back to 1.0 p.u. in a period of 0.33 s. However, in this test, it is assumed that the load under consideration has a voltage stabilizer in the front end. Therefore, the load current will almost not feel any changes in the supply voltage.

At the tenth cycle when there is a sudden sag in the supply voltage, the

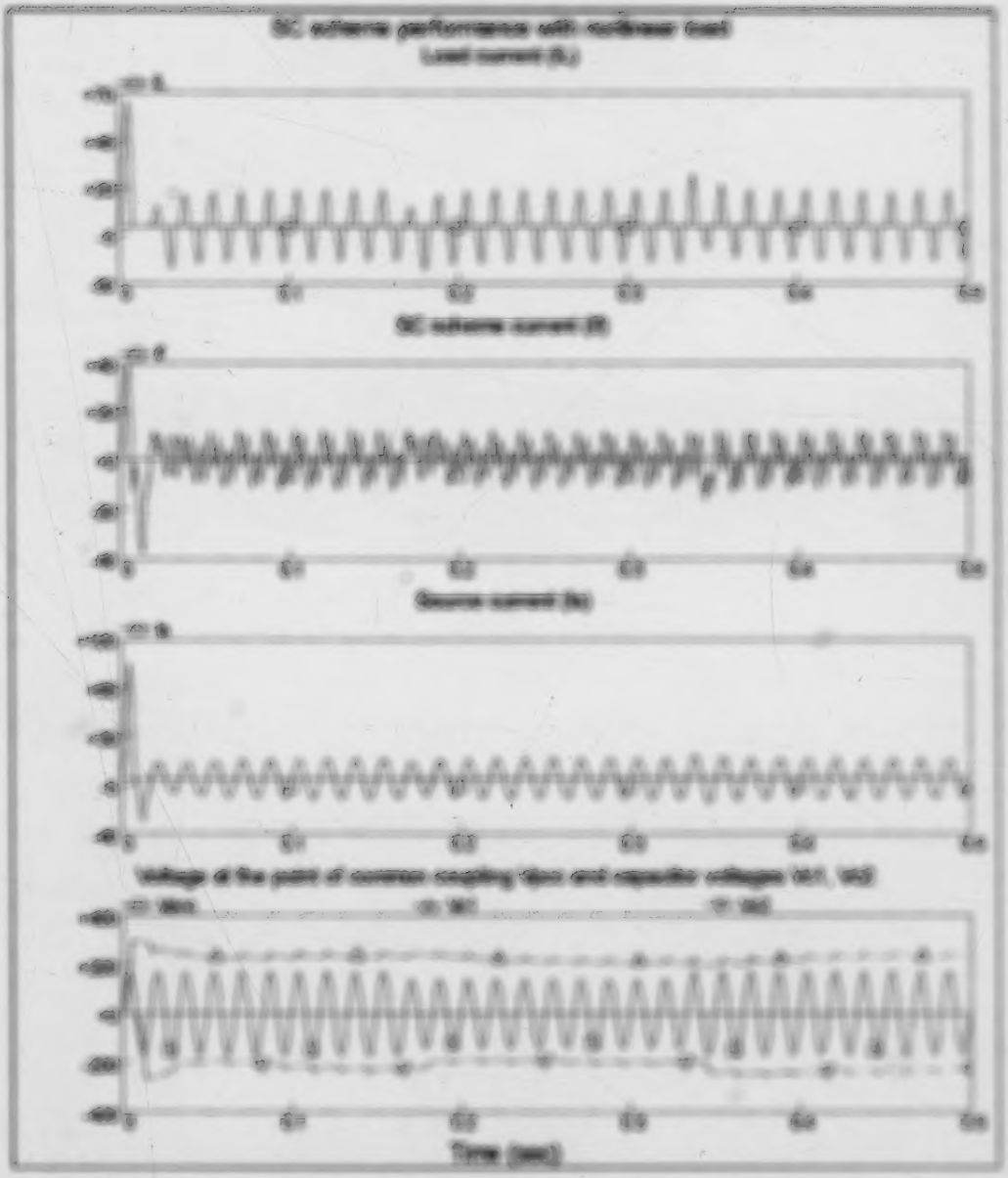

SC scheme performance with nonlinear load
Load current (iL)
SC scheme current (ifil)
Source current (is)
Voltage at the point of common coupling Vpcc and capacitor voltages (Vc1, Vc2)
Time (sec)

Figure 5.14 Simulation results for transient response of the SC filter for a step increase and decrease in the v_{pcc} at the tenth cycle and twentieth cycle respectively with a constant load current.

a- Load current,

b- Filter Current,

c- Source current,

d- v_{pcc}, v_{c1} & v_{c2}

capacitor voltage starts to decrease and stabilizes at a value below the reference one as explained in the previous section. The only difference in the capacitor voltage in this case is the maximum (minimum) capacitor voltage that is slightly higher (lower) than the one in the previous section. This is due to the bigger current provided by the SC filter that increases the ripple in the capacitor voltage. However, that filter could still provide a current that maintains a sinusoidal supply current. Further, the capacitor voltage could respond immediately to cope with the supply voltage changes, and to maintain a sinusoidal ac main current.

5.5 Experimental Set Up

In order to confirm the accuracy of the simulation and to investigate the real performance of the SC filter, the power circuit configuration and the control system hardware of the experimental proto type is described in this chapter.

5.5.1 Power and Control Circuits

The power and control circuits used in this section are the same circuits used in the previous chapter with minor differences as follows:

- *Power Circuit*: the critical Load is a 5.0 % reactor is used in the ac side a non-linear load. The non-linear load is modeled as a diode rectifier bridge consisting of the following values: (R_L = 22.0 Ω, C_{dc} = 940 μF) and (R_L = 5.0 Ω, L_L = 50 mH).
- *Control Circuit*: the difference is in the reference generation sub circuit that is done using UAF technique as shown in figure 5.15

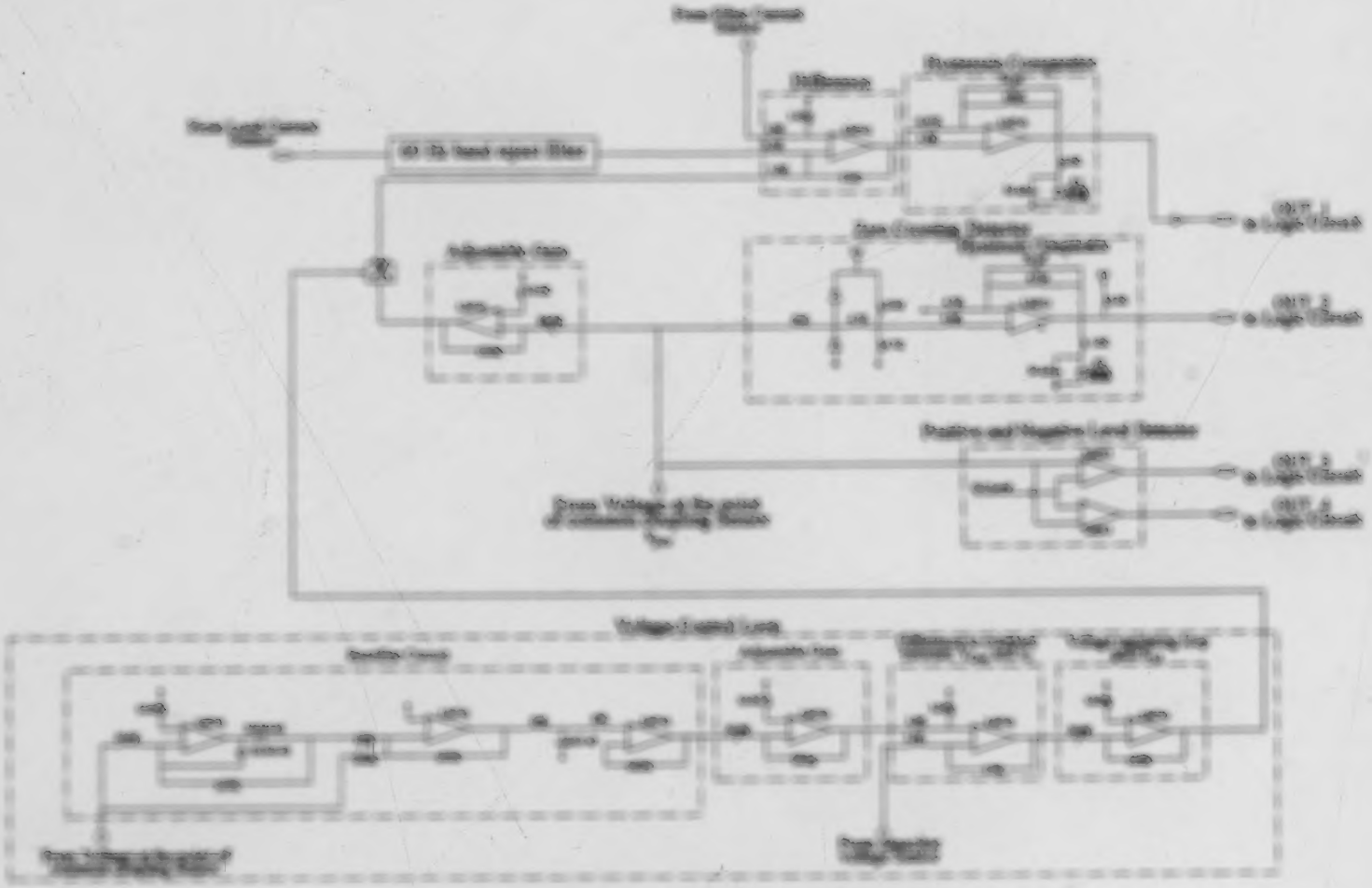


Figure 3.13 Control circuit hardware

5.5.2 Experimental results

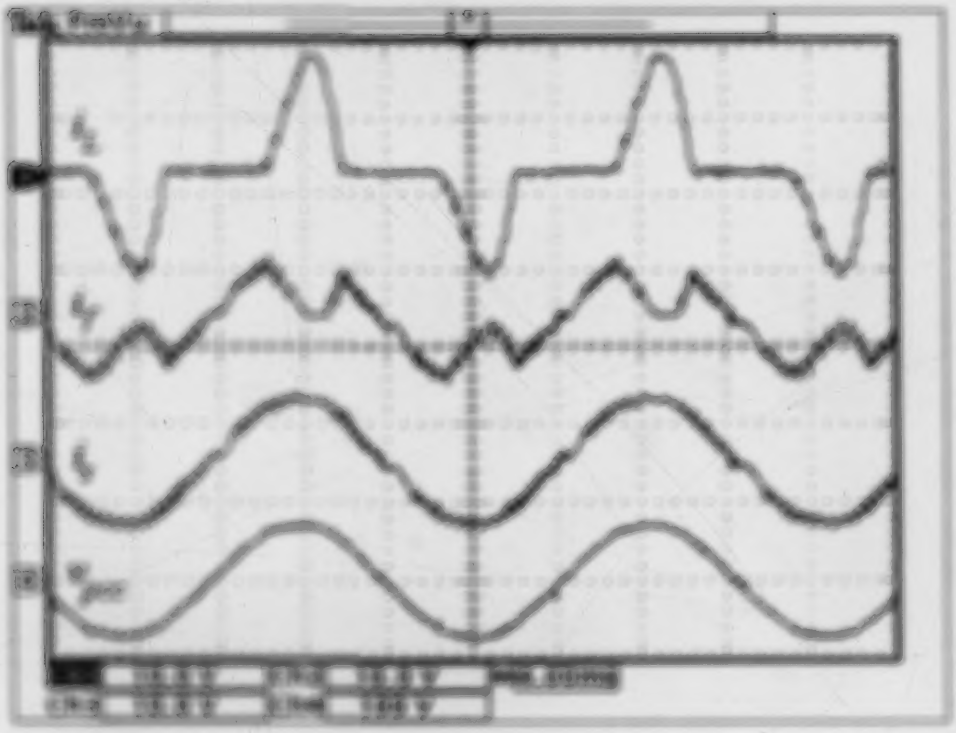
5.5.2.1 Steady state

Figures (5.16-5.18) document the results of the laboratory set-up for two non-linear loads under study.

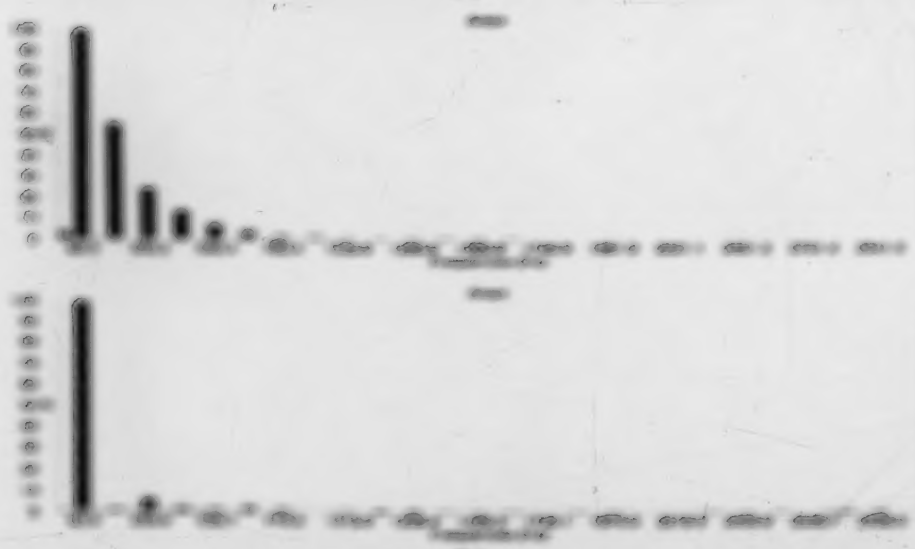
Figure 5.16a shows the practical results of the load current, filter current, source current, and voltage at the point of common coupling for a single-phase bridge rectifier with a capacitive filter that has a THID of 99%. The scheme can significantly decrease the THID of the source current to 5.3%. Furthermore, the current spectrum for the load and source, shown in figure 5.16b, shows the great effect of the filter in reducing the 3^{rd}, 5^{th}, and 7^{th} harmonics. An even lower THID can be obtained by decreasing the hysteresis window at the expense of higher switching losses.

The capacitor voltage waveforms, v_{c1} and v_{c2}, along with the v_{pcc} and DC filter current are shown in figure 5.17 for the capacitor filter load case. One can see that the capacitor voltages are always maintained at a level higher than v_{pcc} that allow the filter to perform its function properly.

Finally, similar results for a single-phase rectifier bridge with an inductive load are shown in figure 5.18 where the THID could be improved from 27% at the load side to 4.7% at the source side.



(a)



(b)

Figure 7: (a Load current, (b) filter current, supply current and voltage at the point of common coupling with rectifier bridge with capacitive filter load, (b) Harmonic spectrum for both load and supply currents

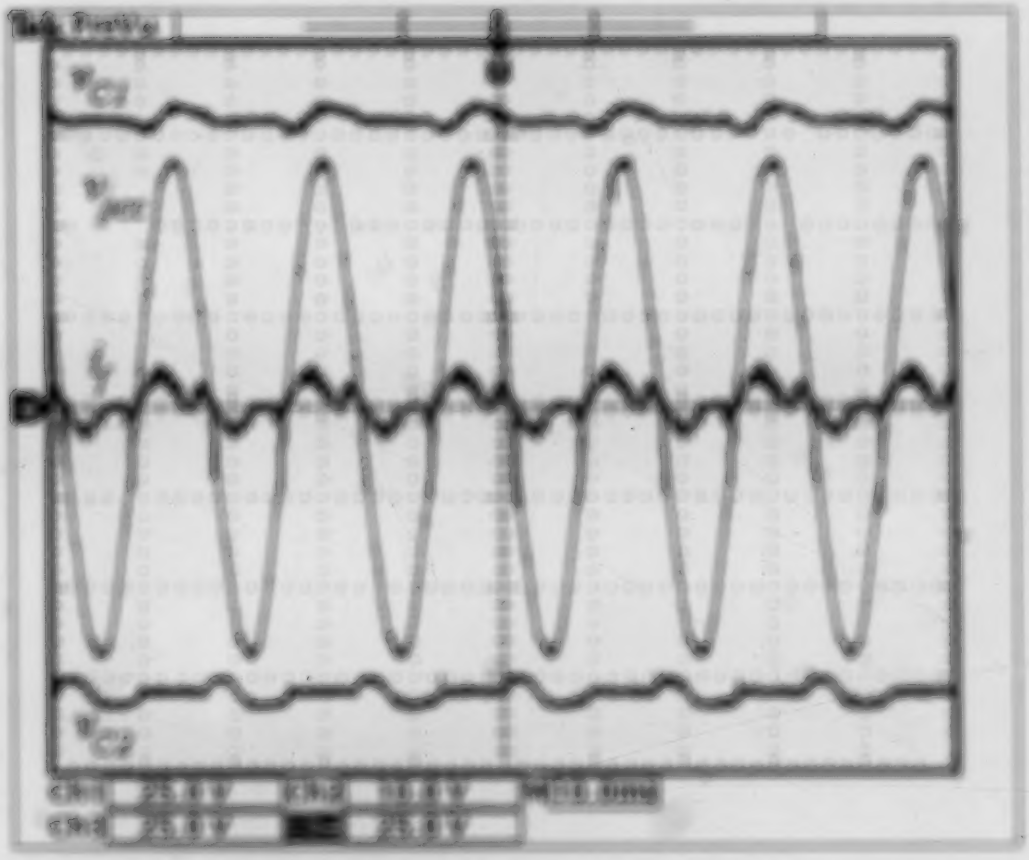
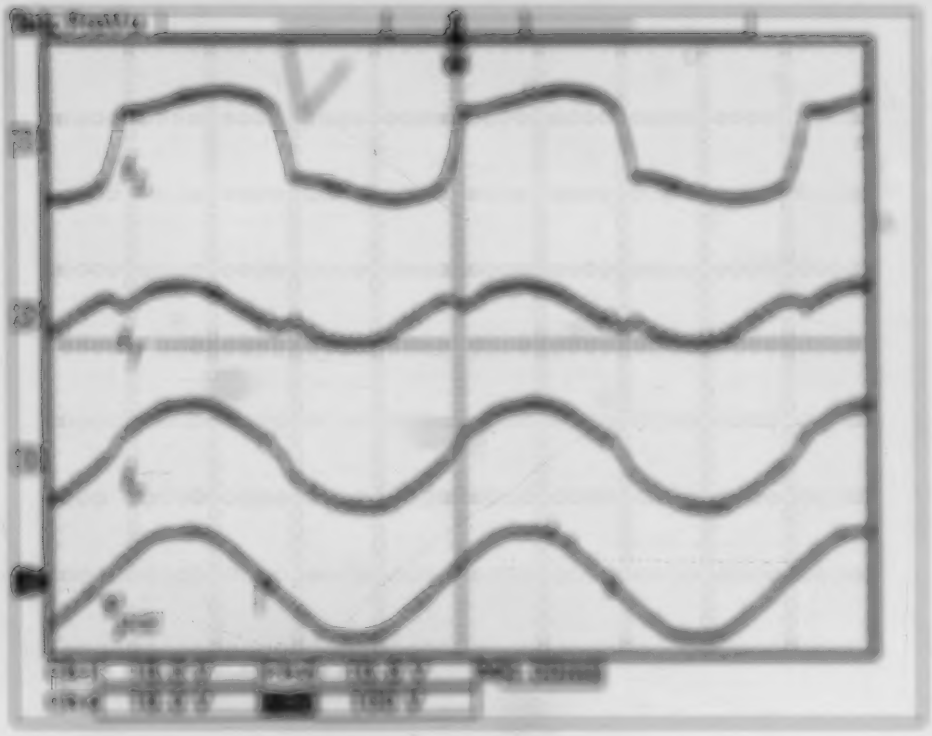


Figure 5.17 Experimental waveforms for the voltage v_{pn}, capacitor voltages v_{C1} & v_{C2} and DC filter current i_f



(a)

(b)

Figure 1.19 (a) Load current, (i_L) filter current, supply current and voltage at the point of common coupling with rectifier bridge with inductive load, (b) Harmonic spectrum for both load and supply current.

(d)

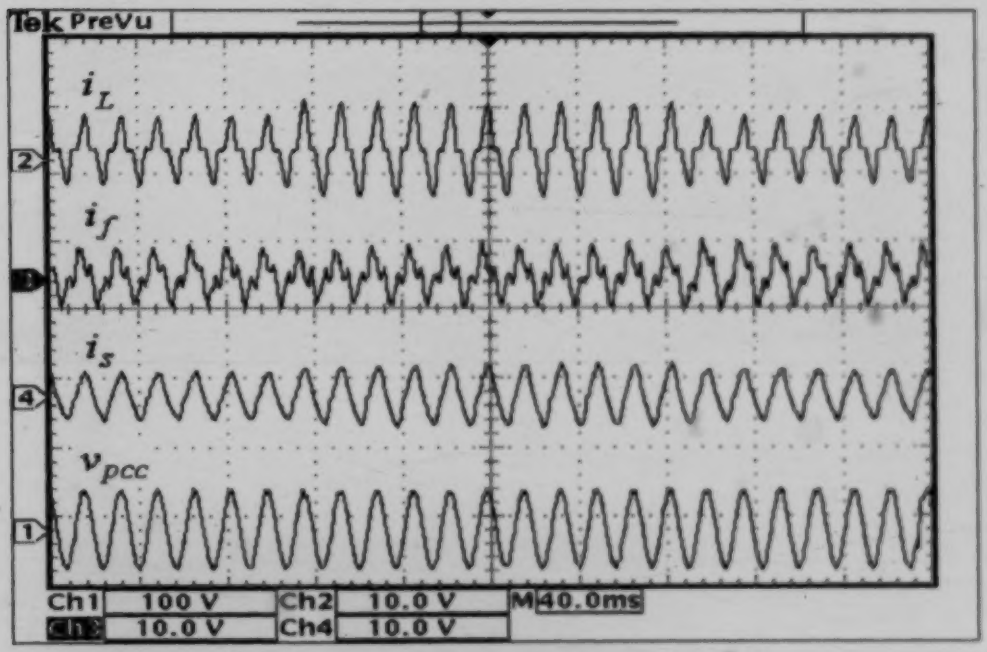
4.3.3.3 Transient analysis

Figures 4.19 (a-c) and 4.20 demonstrate the performance of the SC based active filter under two different transient analyses, which are load current variation and source voltage variation. The load under consideration is a bridge rectifier with capacitive filter.

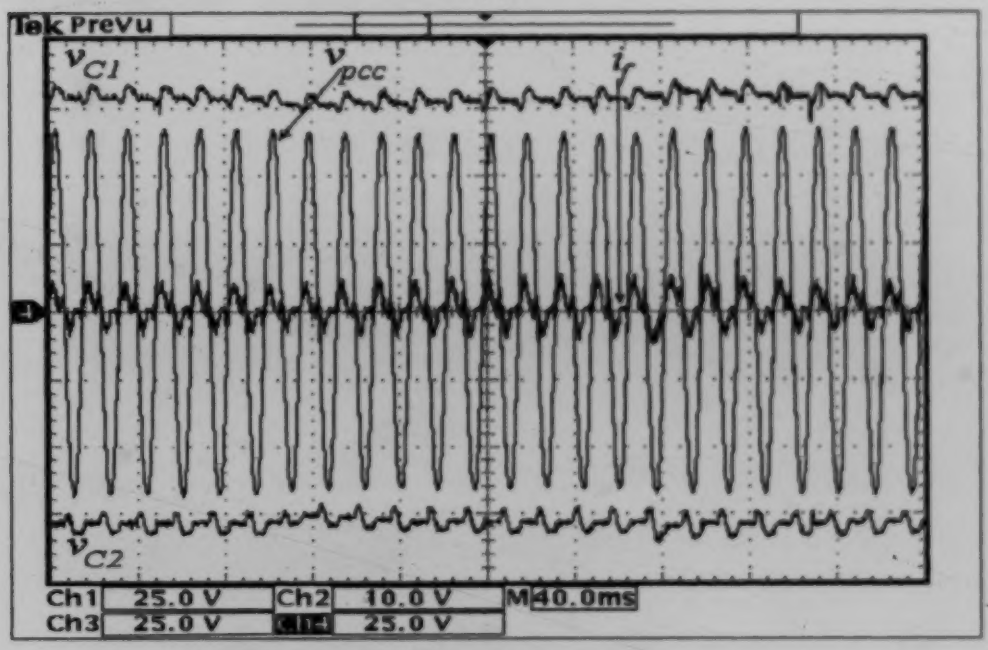
The waveforms in figure 4.19a show the response of the SC active filter when load current changes in a step-like manner from 0.5 p.u. to 0.8 p.u. and back to 0.5 p.u. in a period of 0.04 s. The waveforms reveals that the SC scheme responds very fast to the load variation and maintains a sinusoidal source current all the time. This is rather confirmed from the capacitor voltage variation in figure 4.19b that dropped slightly from its reference due to the fast change in the load current that results in a small active current to flow in the capacitor. However, the figure shows that the capacitor voltage could attain its required voltage value in a fair manner due to the operation of the voltage regulating loop that allow the SC scheme to perform its function correctly.

Finally, figure 4.20 shows the response of the SC scheme when the supply voltage changes in a step-like manner from 1.0 p.u. to 0.7 p.u. and back to 1.0 p.u. in a period of 0.04 s.

In figure 4.20a, one can see that the SC scheme could effectively deliver the required harmonic current during voltage sags to compensate for the distortion in the system. One can further conclude from figure 4.20b that the voltage regulation loop could effectively maintain the capacitor voltage at a level that is higher than the supply voltage to allow the SC scheme to perform its function properly.



(a)

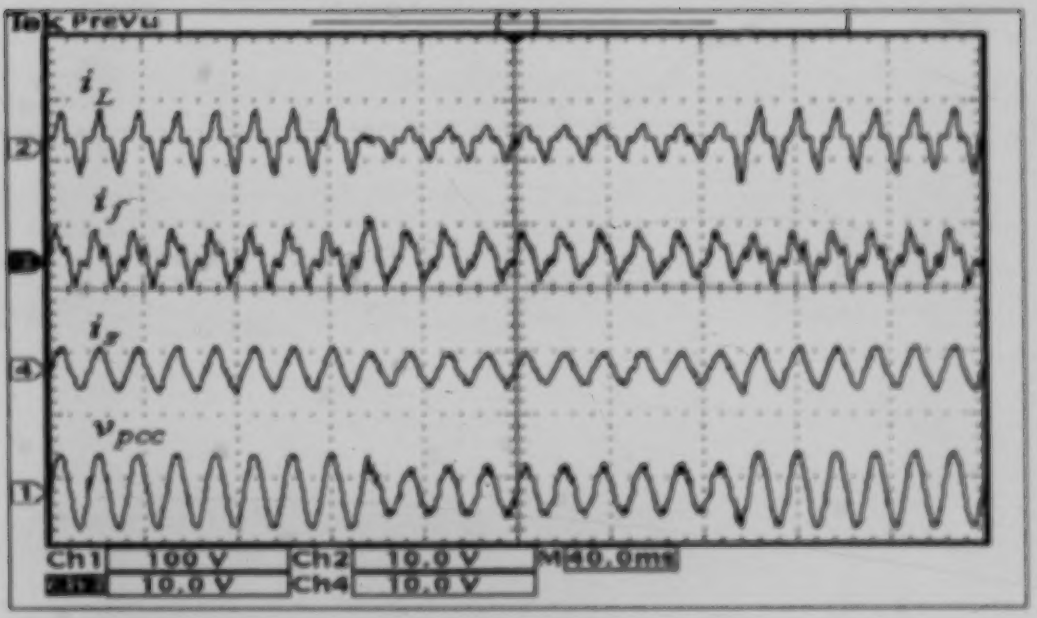


(b)

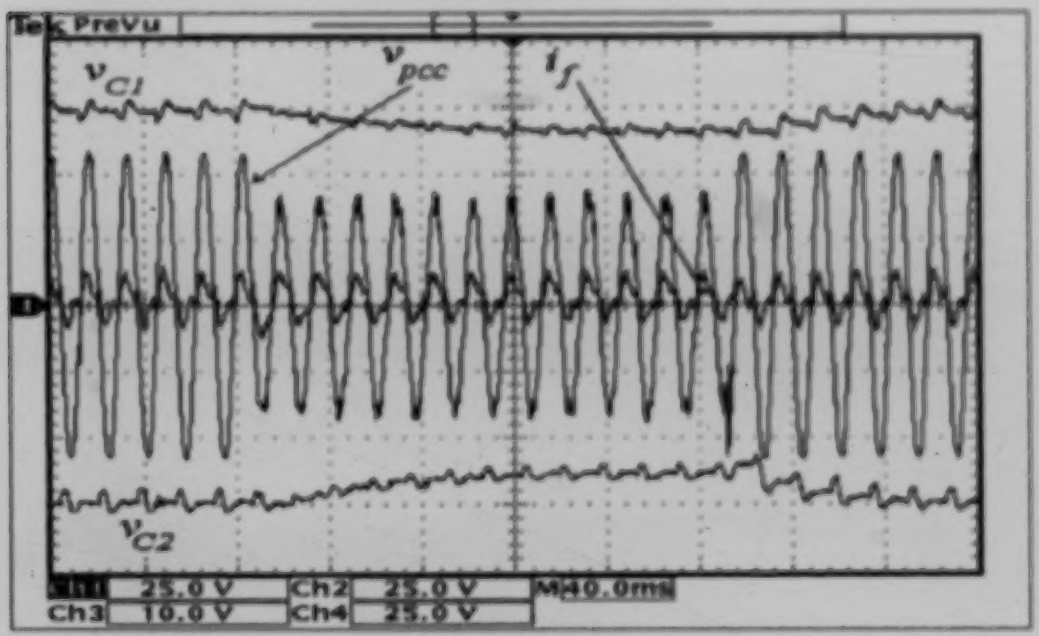
Figure 5.19 SC scheme performance for a cyclic load current variation.

(a) i_L, i_f, i_s *and* v_{pcc}.

(b) v_{pcc}, v_{c1} & v_{c2} *and* i_f.



(a)



(b)

Figure 5.20 SC scheme performance for a cyclic supply voltage variation.

(a) i_L, i_S, i_z and v_{pcc}.

(b) v_{pcc}, v_{c1} & v_{c2} and i_f.

5.6 Conclusions

This chapter has presented a complete design for the SC scheme when operating as active power filter. The design includes the control circuit and passive components selection. The chapter has further presented some simulation results to evaluate the performance of the SC filter under steady state and transient operations to verify the effectiveness of the SC scheme and the design methodology used.

- First, since the SC scheme does not include large storage elements, the net active power flow in the compensator should be minimum in steady state to maintain the capacitor voltages at the required level. Therefore, two detection methods, UAF and ANC, that are easy to implement and can provide the reference current with fast response, are chosen for generating the reference current for compensating harmonic currents for a given load.
- The simulation is performed with the PSCAD software program using both the UAF and ANC techniques to have a complete overview of the performance of the SC scheme under different reference generation circuits that assist the choice of UAF circuit that is easy to implement, cost effective, and easy to adjust, which makes it more suitable for our application.
- It is also shown that the SC active power filter can successfully compensate for non-linear loads with a fast speed of response for reference current and supply voltage variations resulting in a source current with minor harmonic components.

Finally, the simulation and experimental results demonstrated that significant harmonic mitigation could be obtained with an average switching frequency as low as 3.0 kHz.

CHAPTER 6

Conclusions and Future Work

The scheme, control circuit and design approach for the SC power conditioner proposed in this work has been shown to be viable. With this approach, the basic parameters, which control the characteristics of the power conditioner, are easily identified, thereby providing a useful procedure for selection of suitable parameters for different applications. The main features of this approach are summarized in this chapter. Finally, during the course of this research, some possible topics for future work in this area have been detected and are listed at the end of this chapter.

6.1 Conclusions

The results of this study including the design, analysis, simulation and experimental work of the proposed SC scheme are summarized as follows:

- A new single-phase topology which is based on switched capacitor technology and which can be used for reactive power compensation and harmonic mitigation is presented having the following merits:
  - It presents a simple power structure; only three bi-directional switches and two small capacitors,
  - can be controlled with standard hysteresis current control,
  - operates with low switching frequency,
  - has small passive elements, and
  - has fast transient response.

- A systematic design procedure, which is based on a detailed code for simulating currents and voltages in the proposed SC circuit and an optimization technique, is provided for the choice of the system components for different loads. The validity of the design procedure is verified by means of simulation analysis, with PSCAD software, and experimental work with a laboratory prototype. The results of both the simulation and experimental works very closely agree with the results obtained from the curves resulting from the design optimization, which proves the effectiveness of the design technique.

- The control methodology of the power conditioner is one of the key elements for enhancing its performance for reactive power compensation and harmonic mitigation. Power quality conditioning can be performed in the time domain or in the frequency domain. Instantaneous Reactive Power Theory (IRP), Frequency Domain Analysis, and d-q Reference Frame Theory are commonly used but they have the inherent disadvantages that they are complex to implement, difficult to adjust, or have relatively long delay times. Moreover, since dynamic compensation requires rapid

detection of the required signal, a control circuit that is based on analog components is better than digital detection that is not as fast. Therefore, a detection technique that is based on Adaptive Noise Canceling (ANC) is chosen for generating the reference current for compensating reactive and harmonic currents for a given load. The detection technique provides excellent accuracy and convergence speed in tracking the fundamental frequency and the harmonic components. Further, it is highly adaptive and is capable of estimating the variations in the fundamental frequency and harmonic components in a fast manner.

- Nevertheless, the standard control strategy presents some drawbacks which limit the operation of the SC scheme such as:
  - the current poor tracking capability of the scheme at the worst possible case for switched capacitor topologies: the zero crossing points of the ac line voltage,
  - and the uncontrolled capacitor voltages.

  Although these limitations have a negative effect of adding some distortion to the source current waveform, the SC scheme could provide dynamic inductive, capacitive and harmonic currents to compensate for reactive currents and harmonics distortion that have been verified with simulation and experimental results.

- To improve the performance of the proposed SC scheme, a modified control strategy for the standard hysteresis control is proposed which can:
  - provide an alternative switching scheme for hysteresis control that allows an increase in the current tracking capability of the scheme around the zero crossing points of the AC line voltage, and
  - keep the capacitor voltages at certain required level by adding a voltage control loop, which allows proper operation of the SC scheme with small capacitor sizes.

- For the compensator operating as an SVC independent of the load, it was shown that it presents a fast speed of response for reference current variations and that it can

keep close track of the reference current for sudden variations in the PCC voltage. Moreover, it was shown that the proposed switched capacitor converter can successfully compensate for variations of linear and non-linear loads resulting in a source current with minor harmonic components and in phase with the fundamental voltage. Further, the simulation and experimental results demonstrated that significant harmonic mitigation can be obtained with an average switching frequency as low as 3.0 kHz. Finally, to better evaluate the proposed SC scheme, a comparison between the proposed SC scheme and the single-phase inverter based power conditioner from the installation cost point of view is provided which proved that the proposed SC power conditioner can reduce the total cost significantly by almost 50% when compared with the inverter-based scheme for the same kind of applications.

- For high power applications, the main aim of proposed SC circuit is to eliminate or reduce the current harmonics. Because of economic considerations, reactive power compensation using active filters at the high voltage distribution level is not generally regarded as viable, because of the high voltage and its accompanying problems of isolation and series/parallel connections of switches. This way the rating of the power conditioner will be reduced significantly. Therefore, a complete design for the SC scheme when operating as an active power filter is presented. The design includes the control circuit and passive components selection. A reference generation circuit, which is based on UAF technique, is chosen, as it is easy to implement, cost effective, and easy to adjust, which makes it more suitable for this application. It is also shown that the SC active power filter can successfully compensate for non-linear loads with a fast speed of response for reference current and supply voltage variations resulting in a source current with minor harmonic components. Finally, the experimental results confirm the observation concluded from the simulation and show the performance of the SC scheme for different loading conditions.

- Finally, while the experimental work was based on low voltage and low power system, the principle outlined is applicable to high voltage and power ratings provided that suitable switches are available.

6.2 Suggestions for Future Work

6.2.1 Application of the SC Scheme for Three Phase System

None of the researchers had proposed a three phase active filter that is based on the SC technology. Further, the SC scheme proposed in the current work still aims to solve the problems of reactive power compensation and harmonic mitigation in single-phase applications.

This section proposes a three-phase active filter scheme that is based on switched capacitor technology. The scheme is using two single-phase SC based compensator topology as shown in figure 6.1 instead of controlling the three phases separately [3,95], two single-phase units can do the same function. Further, this way the number of switches will be reduced from nine to six for this kind of schemes or from twelve to six if using three single-phase inverter bridges. The scheme is based on the sum of the current in a three phase three-wire system is zero:

$$i_a + i_b + i_c = 0 \qquad (6.1)$$

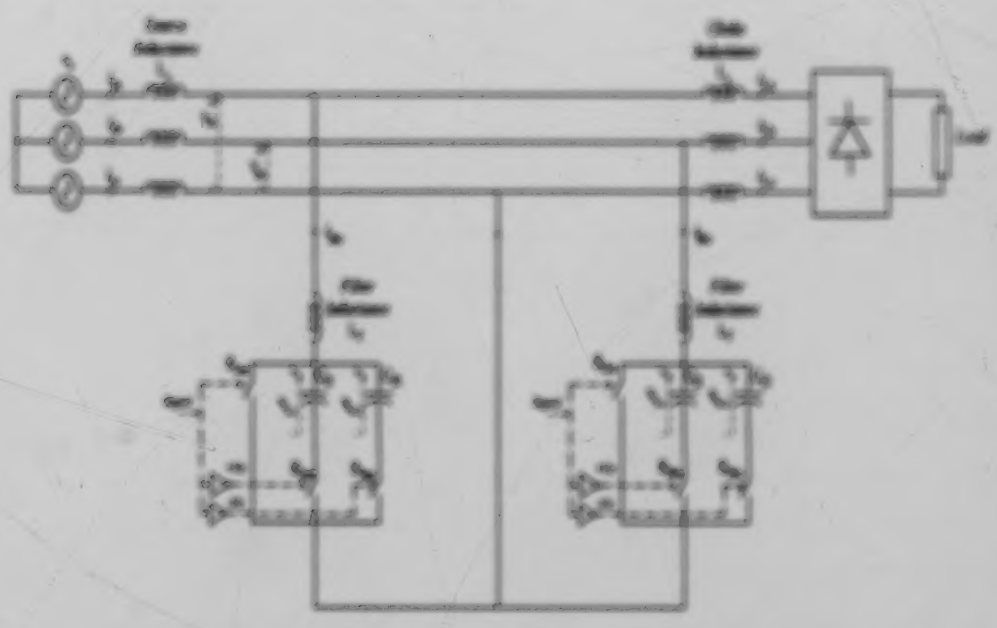


Figure 6.1 System configuration of the proposed active filter scheme

Therefore, if i_c, & i_b are controlled to be sinusoidal and free of harmonics, i_a will consequently become sinusoidal. Consequently, the first unit controls the current that goes through phase 'a' and the return path will be phase 'c' and the second unit controls the current that goes through phase 'b' and the return path will be again phase 'c'. This way the three line currents are controlled at the same time. The line current of the power conditioner can be made to follow a given reference by controlling its rate of change which can be made either positive or negative depending on what switch is "ON". As a matter of fact, the coil voltage $(v_{L,ab} = L\, di/dt)$ determines the slope of the current. As long as the capacitor voltages are bigger than their respective line-line voltages, $|v_{C1,2}| > |v_{L,2}|$ at all times, the slope of the current is the same as the polarity of $v_{L,2}$ when S_1 is on (mode 1) and the opposite when either S_2 or S_3 are on (mode 2). The magnitude of the rate of change of the current in the inductor for the two modes can be calculated as follows:

$$\frac{di_L}{dt} = \frac{v_{L,2}}{L_f} \quad \& \quad \frac{di_L}{dt} = \frac{v_{L,2} - \delta v_C}{L_f} \tag{6.2}$$

Where $\delta = 1$ if $v_{L,2} > 0$, and $\delta = -1$ if $v_{L,2} < 0$.

Figure 6.2 and figure 6.3 show waveforms for two non-linear loads. A hysteresis window of 5% of the rated peak harmonic current (i_{Lf}) has been used in the simulation. The source current waveform reveals that the filter is effective in compensating for load harmonic current and reducing the total harmonic distortion of the source current from 29.5% to about 3.3 % in phase 'a', 3.2% in phase 'b', and 6.1% in phase 'c', when employing the first load. The THD distortion in phase 'c' is higher than the other phases as both the harmonic distortion in phase 'a' and 'b' are added up in this phase. Similar results are obtained for the second load as the source current THD could be reduced from 21% to almost 3%.

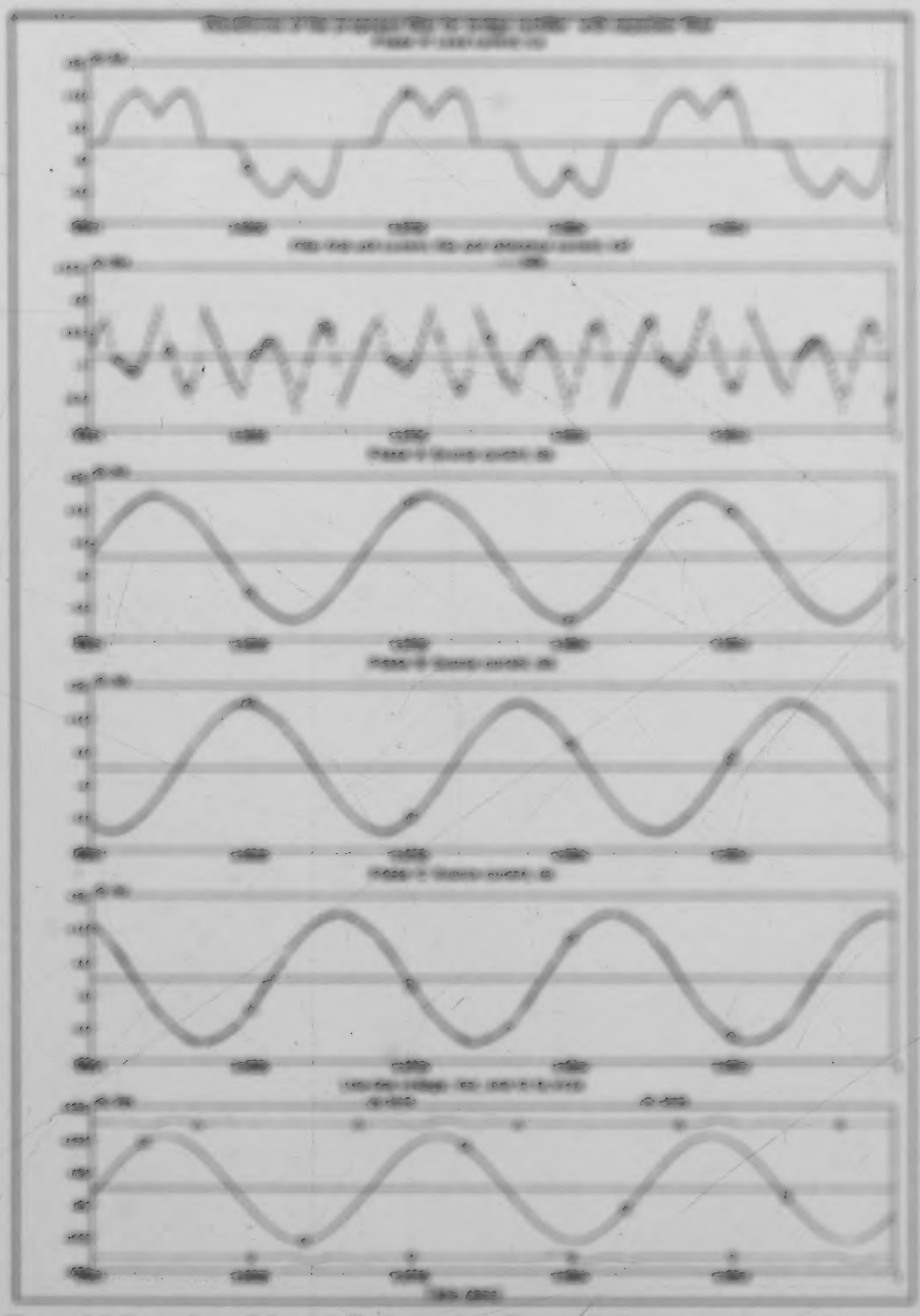


Figure 6.2 Operation of the switched capacitive filter with the proposed control strategy for a diode bridge rectifier with capacitive filter load.

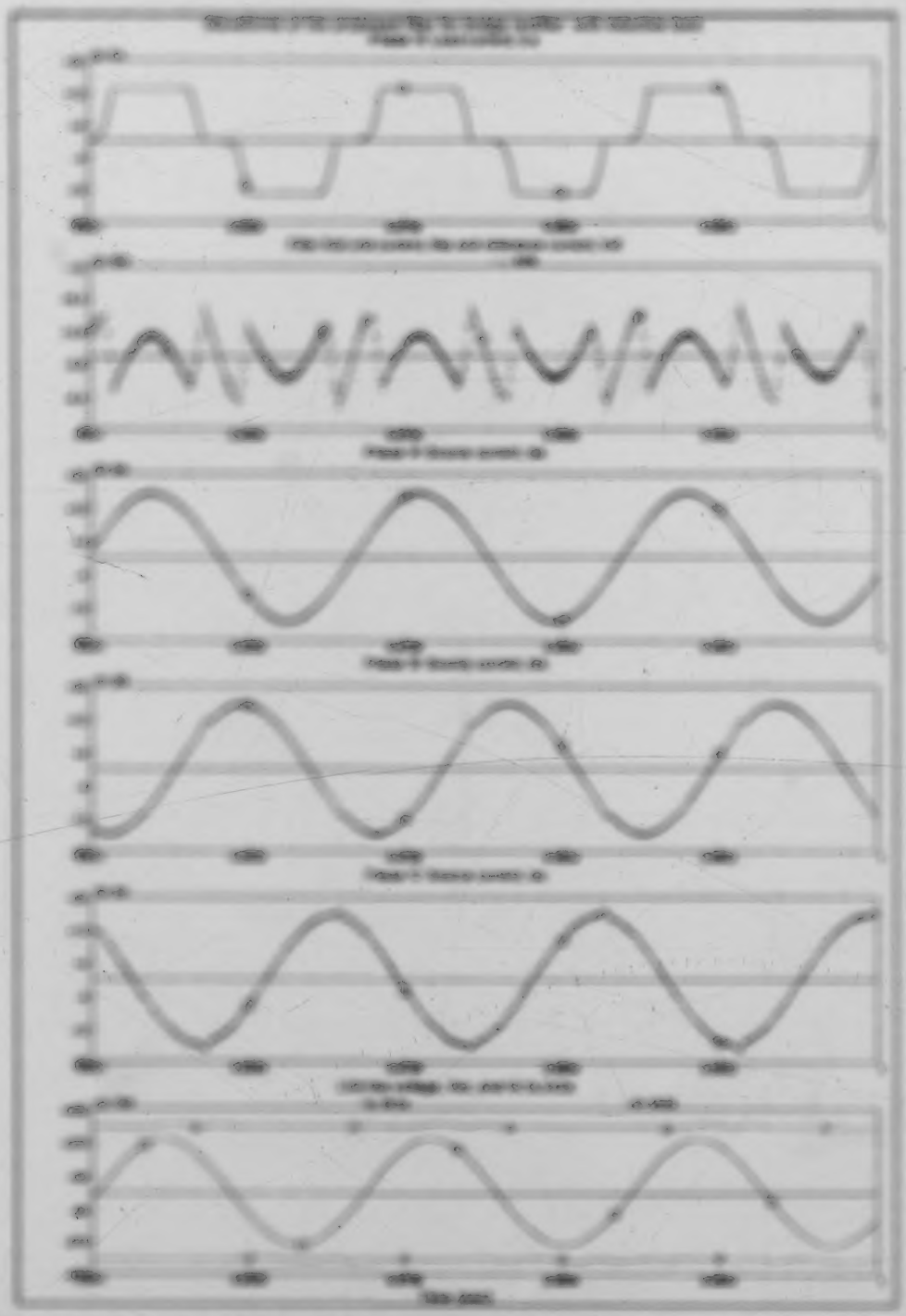


Figure 6.1 Operation of the switched capacitor filter with the proposed control strategy for a diode bridge rectifier with inductive load.

6.2.2 Application of the SC Scheme for Series Compensation

The SC scheme proposed in this work is equally applicable to the construction of active filters for control of voltage harmonics in power systems. Recently, a combined system of shunt passive and series active filter has been proposed by several authors [3,46, 71]. Figure 6.4 illustrates a general diagram of series active filtering technique. The series active filter is controlled to present low impedance at the fundamental frequency and high resistance to the supply and load harmonics.

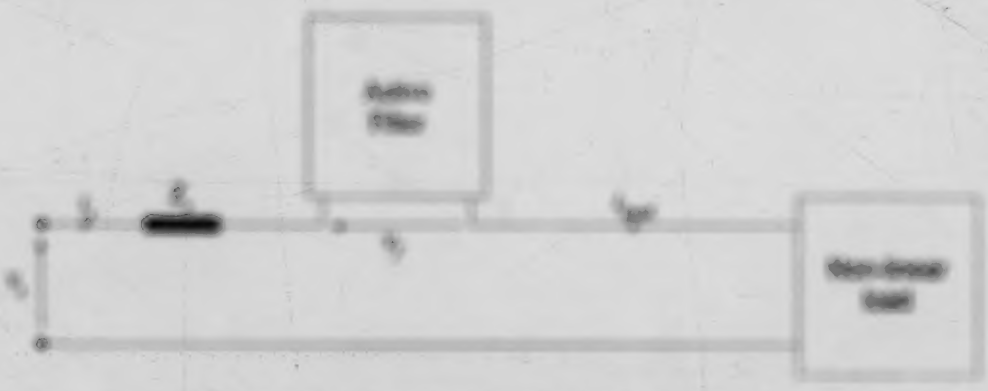


Figure 6.4 Principle of series active filter technique

6.2.3 Other Suggested Future Research Topics

- Operation of the proposed SC scheme under flicker should be investigated.
- Operation of the SC scheme under unbalanced grid voltage and for unbalanced load.

Bibliography

[1] C. Wen, M. Chang, and S. Cen, "Designing passive LC filters with minimax ripple", *Proceedings of the International Conference on Power Electronics and Drive Systems, Singapore*, vol. 2, pp. 814-818, May 1997.

[2] B. Singh, K. Al-Haddad, and A. Chandra, "Review of active filters for power quality improvement", *IEEE Transactions on Industrial Electronics*, vol. 46, pp. 960-971, Oct. 1999.

[3] M. Depenbrock, D. Navarro and L. Wrona, "Series active power filter based on a sinusoidal current-controlled voltage-source inverter", *IEEE Transactions on Industrial Electronics*, vol. 44, pp. 613-618, Oct. 1997.

[4] D. Rivas, V. S. Ramsden, and P.R. Wilcox, "Hybrid filter control system with adaptive filters for selective elimination of harmonics and interharmonics", *IEE Proceedings of Electric Power Applications*, vol. 147, pp. 299-303, May 2000.

[5] A.E. Emanuel, P.G. Garcia, R. Collantes, T. Gruzen, and J. Rutsella, "Comparison of thyristor-controlled reactors and voltage-source inverters for compensation of flicker caused by arc furnaces", *IEEE Transactions on Power Delivery*, vol. 15, pp. 1025-1031, Oct. 2000.

[6] M. Takeda and T. Wakefield, "A new method to eliminate an harmonic currents by magnetic flux compensation-consideration on basic design", *IEEE Transactions on Power Apparatus and Systems*, 1971.

[7] L. Gyugyi and E. C. Strycula, "Active power filters", *IEEE/IAS Conference Proceedings*, pp. 529-535, 1976.

[8] H. Akagi, A. Nabae, and S. Atoh, "Control strategy of active power filters using multiple voltage source PWM converters", *IEEE Transactions on Industry Applications*, vol. 22, pp. 460-465, 1986.

[9] M. Rukonuzzaman and M. Nakaoka, "A practical approach to harmonic compensation in power systems-series connection of passive and active filters", *IEEE/IAS Conference Proceedings*, pp. 1107-1113, 1998.

[11] B. Singh, and S. Gairola, "A multilevel rectifying system including double-series capacitor-connected diode-rectifier and series-active filter", *IEEE Trans.*, vol. 126, no. 1, pp. 65-80, 1997.

[12] G. Bhuvaneshwari, G. Nagaraj, and B. Banerjee, "Control and reduction of terminal voltage total harmonic distortion (THD) in hybrid series-active parallel-passive filter system", *Proceedings of Power Electronics Specialists Conference (PESC '04)*, pp. 779-784, 2004.

[13] A.R. Chattopadhyay and A.K. Gogoswami, "Current regulated converter design and implementation as a VAR controller and an active filter", *Conference Record of the 1997 IEEE Industry Applications 32nd IAS Annual Meeting*, vol. 1, pp.709-716, 1997.

[14] M. El-Habrouk, M.K. Darwish, and P. Mehta, "Active power filters: A review", *IEE Proceedings of Electric Power Applications*, vol. 147, no. 5, pp.403-413, Sep 2000.

[15] B. Singh, B. Singh, and M. Bhuwa, "A multilevel rectifying system including double-series capacitor-connected diode-rectifier and series-active filter", *IEE Trans.*, vol. 126, pp. 65-80, 1997.

[16] M. El-Habrouk and M.K. Darwish, "A new control technique for active power filters using a combined genetic algorithm/conventional analysis", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 1, pp.58-65, Feb 2002.

[17] M.M. Elias and E. Pollack, "Series compensation on power system with very low harmonic distortion", *IEEE Transactions on Power Delivery*, vol. 14, no. 3, pp.1123-1128, Apr 1999.

[18] A.R. Chattopadhyay and A.K. Gogoswami, "Current regulated controlled capacitor static var compensator", *IEEE Transactions on Industry Applications*, vol. 33, no. 6, pp. 1564-1567, July-Aug 1997.

[19] D. Shevitski, D. Czarkowski, and Z. Zabar, "Sine switch-mode topology for VAR compensation", *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '99)*, vol. 5, pp. 56-131, 1999.

[20] S. Ghosh and S. Van Wyk, "Measurement and compensation of fictitious power under nonsinusoidal voltage and current conditions", *IEEE Transactions on Instrumentation and Measurement*, vol. 37, no. 3, pp. 403-408, 1988.

[20] J. Enslin and J. Van Wyk, "A new control philosophy for power electronic converters as fictitious power compensators", *IEEE Transactions on Power Electronics*, vol. 5, no. 1, pp. 88-97, 1990.

[21] G. Van Harmelen and J. Enslin, "Real time dynamic control of dynamic power filters in supplies with high contamination", *IEEE Transactions on Power Electronics*, vol. 8, no. 3, pp. 301-308, 1993.

[22] C. Hsu and H. Wu, "A new single phase active power filter with reduced energy storage capacity", *IEE Proceedings of Electric Power Applications*, vol. 143, no. 1, pp. 25-30, 1996.

[23] J. Rodriguez, E. Wiechmann, E. Suarez, and A. Barria "A contribution to the control of a single phase active power filter", *Proceedings of Brazilian Power Electronics Conference (COBEP-93), Brazil*, pp. 58-64, 1993.

[24] D. Torrey and M. Al-Zamel, "Single phase active power filters for multiple non-linear loads", *IEEE Transactions on Power Electronics*, vol. 10, no. 3, pp. 263-272, 1995.

[25] M. Machmoum, N. Bruyant, and S. Siala, "A practical approach to harmonic current compensation by single phase active filter", *Proceedings of European Power Electronics Conference (EPE-95)*, Spain, pp. 505-510, 1995.

[26] J. Nastran, R. Cajhen, M. Seliger, and P. Jereb, "Active power filter for non-linear ac loads", *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 92-96, 1994.

[27] G. Choe and M. Park, "Analysis and design of active power filter with optimized injection", *IEEE Transactions on Power Electronics*, vol. 4, no. 4, pp. 427-433, 1989.

[28] V. Bhavaraju P. Enjeti, "A fast active power filter to correct line voltage sags", *IEEE Transactions on Industrial Electronics*, vol. 41, no.3, pp. 333-338, 1994.

[29] P. Mehta, M. Darwish, and T. Tomson, "Switched capacitor filters", *IEEE Transactions on Power Electronics*, vol. 5, no. 3, pp. 331-336, 1990.

[30] Z. Koozehkanani, P. Mehta, and M. Darwish, "Active filter for eliminating current harmonics caused by non-linear circuit elements", *Electronic Letter*, vol. 31, no. 13, pp. 1041-1042, 1995.

[31] Z. Koozehkanani, P. Mehta, and M. Darwish, "Active symmetrical lattice filter for harmonic current reduction", *Proceedings of European Power Electronics Conference (EPE-95)*, Spain, pp. 869-873, 1995.

[32] W. Koczara, S. Greetham, and L. Haydock, "An investigation of the reduction of harmonics an reactive power in a single phase system using an adaptive filter", *Proceedings of Power Electronics and Motion Control Conference (PEMC94)*, Poland, pp. 196-201, 1994.

[33] M. El_Habrouk, M. Darwish P. Mehta, "A new configuration for shunt active filters", *Proceedings of European Power Electronics Conference (EPE-97)*, Norway, pp. 4.892-4.897, 1997.

[34] D. Koval and C. Carter, "Power Quality Characterization of Computer Loads", *IEEE Transactions on Industry Applications*, vol. 33, no. 3, pp. 613, 1997.

[35] J. Arrilaga, B. Smith, N. Watson, and A. Wood, "Power system harmonic analysis", John Wiley and Sons, 1985.

[36] IEEE: "Guide for applying harmonic limits on power systems", *P519A Harmonics working group (IEEE PES T&D committee) and SCC22-Power quality*, 1996.

[37] W. Xu, Y. Mansour, C. Siggers, and M. Hughes, "Developing utility harmonic regulations based on IEEE STD-519-B.C. hydro's approach", *IEEE Transactions on Power Delivery*, vol. 10, no. 3, pp. 1423-1431, 1995.

[38] Y. Hayashi, N. Sato, and K. Takahashi, "A novel control of a current source active filter for ac power system harmonic compensation", *IEEE Transactions on Industry Applications*, vol. 27, no. 2, pp. 380-384, 1991.

[39] S. Kim, J. Park, J. Kim, G. Choe, and M. Park, "An improved PWM current control method for harmonic elimination using active power filter", *IEEE Industrial Applications Society Annual Meeting*, pp. 927-931, 1987.

[40] S. Fukuda, and M. Yamaji, "Design and characteristics of active power filter using current source converter", *IEEE Industrial Applications Society Annual Meeting*, pp. 965-970, 1990.

[41] P. Viriya and K. Matsuse, "Low harmonic GTO converter for fundamental power factor correction", *IEEE Transactions on Power Electronics*, vol. 6, no. 3, pp. 371-379, 1991.

[42] G. Cho, G. Jung, and N. Choi, "Analysis and controller design of static var compensator using three level GTO inverter", *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 57-65, 1996.

[43] B. Ooi, and S. Dai, "Series type solid state static var compensator", *IEEE Transactions on Power Electronics*, vol. 8, no. 2, pp. 164-169, 1993.

[44] G. Blajszczak, "Direct method for voltage distortion compensation in power networks by series converter filter", *IEE Proceedings of Electric Power Applications*, vol. 142, no. 5, pp. 308-312, 1995.

[45] R. Harley, B. Rigby, and B. Jennings, "Design of a controlled converter which emulates a series capacitive compensator for long power lines", *Proceedings of Power Electronics and Motion Control Conference (PEMC94)*, Poland, pp. 213-218, 1994.

[46] F. Peng, H. Akagi, and A. Nabae, "Compensation characteristics of the combined system of shunt passive and series active filters", *IEEE Transactions on Industry Applications*, vol. 29, no. 1, pp. 144-152, 1992.

[47] S. Fukuda and T. Endoh, "Control method for a combined active filter system employing a current source converter and a high pass filter", *IEEE Transactions on Industry Applications*, vol. 31, no. 3, pp. 590-597, 1995.

[48] J. Havfner, M. Aredes, and K. Heumann, "Utilization of small rated shunt active power filter for large power systems", *Proceedings of Power Electronics and Motion Control Conference (PEMC94)*, Poland, pp. 190-195, 1994.

[49] L. Malesani, L. Rossetto, and P. Tenti, "Active power filter with hybrid energy storage", *IEEE Transactions on Power Electronics*, vol. 6, no. 3, pp. 392-397, 1991.

[50] G. Goos, L. Moran, and P. Ziogas, "Performance analysis of a PWM inverter var compensator", *IEEE Transactions on Power Electronics*, vol. 6, no. 3, pp. 380-391, 1991.

[51] V. Bhavaraju and P. Enjeti, "Analysis and design of an active power filter for balancing unbalanced loads", *IEEE Transactions on Power Electronics*, vol. 8, no. 4, pp. 640-647, 1993.

[52] T. Furuhashi, S. Okuma, and Y. Uchikawa, "A study on the theory of instantaneous reactive power", *IEEE Transactions on Industrial Electronics*, vol. 37, no. 1, pp. 86-90, 1991.

[53] L. Moran, J. Dixon, and R. Wallace, "A three phase active power filter operating with fixed switching frequency for reactive power and current harmonic compensation", *IEEE Transactions on Industrial Electronics*, vol. 42, no. 5, pp. 402-408, 1995.

[54] S. Hoseini and M. Tarafdar, "The presentation of a new active filter with amplitude modulationof difference wave", *Proceedings of Power Electronics and Motion Control Conference (PEMC94)*, Poland, pp. 231-235, 1994.

[55] S. Williams, and R. Hoft, "Adaptive frequency domain control of PWM switched power line conditioner", *IEEE Transactions on Power Electronics*, vol. 6, no. 4, pp. 665-670, 1991.

[56] G. Ledwich and P. Doulai, "Multiple converter performance and active filtering", *IEEE Transactions on Power Electronics*, vol. 10, no. 3, pp. 273-279, 1995.

[57] H. Fujita, S. Tominaga, and H. Akagi, "Analysis and design of a dc voltage controlled static VAR compensator using quad series voltage source inverter", *IEEE Transactions on Industry Applications*, vol. 32, no. 4, pp. 970-978, 1996.

[58] G. Joos, X. Huang, and B. Ooi, "Direct coupled multi-level cascaded series VAR compensator", *IEEE Industry Applications society meeting*, pp. 1609-1615, 1997.

[59] H. Akagi, "New trends in active filters", *Proceedings of European Power Electronics Conference (EPE-95)*, Spain, pp. 17-26, 1995.

[60] H. Akagi, "New trends in active filters for power conditioning", *IEEE Transactions on Industry Applications*, vol. 32, no. 6, pp. 1312, 1996.

[61] W. Grady, M. Samotyj, and A. Noyola, "Survey of active power line codtioning methodologies", *IEEE Transactions on Power Delivery*, vol. 5, no. 3, pp. 1536-1542, 1990.

[62] M. Aredes, J. Hafner, and K. Heumann, "Three phase four-wire shunt active filter control", *IEEE Transactions on Power Electronics*, vol. 12, no. 2, pp. 311-318, 1997.

[63] A. Cavallini and G. Montanari, "Compensation strategies for shunt active filter control", *IEEE Transactions on Power Electronics*, vol. 9, no. 6, pp. 587-593, 1994.

[64] H. Hou, "Performance comparison of three phase active power filter algorithms", *IEE Proceedings of Generation, Transmission, and Distribution*, vol. 142, no. 6, pp. 646, 1995.

[65] M. Welsh, P. Mehta, and M. Dar..., "Genetic algorithm and extended analysis optimization techniques for switched capacitor active filters- a comparative study", *IEE Proceedings of Electric Power Applications*, vol. 147, no. 1, pp. 21-26, 2000.

[66] M. El-Habrouk and M.K. Darwish, "A new control technique for active power filters using a combined genetic algorithm/conventional analysis", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 1, p 58-66, 2002.

[67] A.K. Chakravorti and A.E. Emanuel, "Current regulated converter: design and limitations as a VAR controller and an active filter", *Conference Record of the 1995 IEEE Industry Applications 30th IAS Annual Meeting*, vol. 3, p 2703-2710, 1995.

[68] T. Kandil, L. Lopes, and Wilsun Xu, "Analysis and Design of a New Current Controlled Switched Capacitor Filter", *Electric Power Components and System Journal.*

[69] S. Bhattacharya, D. Divan, and B. Banerjee, "Control and reduction of terminal voltage total harmonic distortion (THD) in hybrid series-active parallel-passive filter system", *Proceedings of Power Electronics Specialists Conference (PESC'93)*, pp. 779-786, 1993.

[70] Z. Yao, S. Lahaie, and V. Rajagopolan, "Robust compensator of harmonics and reactive power", *Proceedings of Power Electronics Specialists Conference (PESC'95)*, pp. 215-221, 1995.

[71] M. Rastogi, N. Mohan, and A. Edris, "*Hybrid-active filtering of harmonic currents in power systems*", *IEEE Transactions on Power Delivery*, vol. 10, pp. 1994-2000, Apr. 1995.

[72] F. Libano, D. Simonetti, and J. Uceda, "Frequency characteristics of hybrid filter systems ", *Proceedings of Power Electronics Specialists Conference (PESC'96)*, pp. 1142-1148, 1996.

[73] A. Zyl, J. Enslin, W. Steyn, and R. Spee, "A new unfied approach to power quality management", *Proceedings of Power Electronics Specialists Conference (PESC'95)*, pp. 183-188, 1995.

[74] F. Kamran and T. Habetler, "Combined deadbeat control of a series parallel converter combination used as a universal power filter", *Proceedings of Power Electronics Specialists Conference (PESC'95)*, pp. 196-201, 1995.

[75] H. Akagi, "New trends in active filters for improving power quality", *Proceedings of IEEE PEDES'96*, pp. 417-425, 1996.

[76] B. Bird, J. March, and P. Mclellan, "Harmonic reduction in multiplex converter by triple frequency current injection", *IEE Proceedings on Electric Power Applications*, vol. 116, No. 10, pp. 1730-1734, 1969.

[77] W. Grady, M. Samotyj, and A. Noyola, "Survey of active power line conditioning methodologies", *IEEE Transactions on Power Delivery*, vol. 5, pp. 1536-1542, 1990.

[78] S. Bhattacharya, D. Divan, and B. Banerjee, "Active filter solutions for utility interface", *Proceedings of IEEE ISIE'95*, pp. 1-11, 1995.

[79] P. Cheng, S. Bhattacharya, and D. Divan, "Hybrid solutions for improving passive filter performance in high power applications", *Proceedings of IEEE APEC'96*, pp. 911-917, 1996.

[80] Z. Radulovic and A. Sabanovic, "Active filter control using a sliding mode approach", *Proceedings of Power Electronics Specialists Conference (PESC'94)*, pp. 177-182, 1994.

[81] S. Saetieo, R. Devaraj, and D. Torrey, "The design, implementation of a three-phase active power filter based on sliding mode control", *IEEE Transactions on Industry Applications*, vol. 31, pp. 993-1000, 1995.

[82] F.G. Baum, "Voltage regulation and insulation for large power long distance transmission systems," *J. AIEE*, no. 40, pp.1017-1032, 1924.

[83] T. J. E. Miller," Reactive power control in electric systems," New York: Wiley, 1982, Chapter, 6, 241.

[84] M. Chanas, "Perturbations in distribution networks. Compensation by static devices", *Revue Generale D' Electricite*, vol. 87, no. 12, pp. 925-943, Dec. 1978.

[85] S. Bhattacharya, T.M. Frank, D.M. Divan, and B. Banerjee; "Active filter system implementation", *IEEE Industry Applications Magazine*, vol. 4 no. 5, p 47-63, Sep-Oct. 1998.

[86] S. Bhattacharya, D.G. Holmes, and D.M. Divan, "Optimizing three phase current regulators for low inductance loads", *Thirtieth IAS Annual Meeting, IAS '95, Conference Record of the 1995 IEEE*, vol. 3, p 2357-2364, Oct. 1995.

[87] H. Akagi et al., "Generalized theory Instantaneous reactive power and its application," *Electr-Eng-Japan*, vol. 103, pp. 58-66, Jul-Aug 1983.

[88] A. Nakajima et al., "Development of active filter with series resonant circuit," *IEEE-PESC, Annual Meeting*, pp. 1168-1173, 1988.

[89] V. Dinavahi, M. Iravani, and R. Bonert, " Real-time digital simulation of power electronic apparatus interfaced with digital controllers", *IEEE Transactions on Power Delivery*, vol. 16, No. 4, pp. 775-781, Oct. 2001.

[90] Shiguo Luo and Zhenzheng Hou, " An adaptive detecting method for harmonic and reactive currents", *IEEE Transactions on Industrial Electronics*, vol. 42, No. 1, pp. 85-89, Feb. 1995.

[91] Qun Wang, Ning Wu, and Zhaoan Wang, "A neuron adaptive detecting approach of harmonic current for APF and its realization of analog circuit," *IEEE Transactions on Instrumentation and Measurements*, vol.50, No.1, pp. 77-84, 2001.

[92] B. Widrow and S. P. Strens, "Adaptive signal processing", Englewood Cliffs, NJ: Prentice-Hall, Inc., 1985.

[93] D. M. Brod and D. W. Novotny, "Current control of VSI-PWM Inverters", *IEEE Transaction on Industry Application*, IA-21, pp. 562-570, 1985.

[94] Paul Horowitz and Winfield Hill, " The art of electronics", Cambridge [England]; New York: Cambridge University Press, 1989.

[95] F. Libano, J. Cobos, and J. Uceda, "Simplified control strategy for hybrid active filters", *Power Electronics Specialists Conference, PESC '97*, vol. 2, pp. 22-27, 1997.

APPENDIX A

Calculation of the Constants A_{1k} & A_{2k} for the Mathematical Code

To get the filter current at any instant k, the constants A_{1k} & A_{2k} should be calculated. To solve for A_{1k} & A_{2k}, two equations in the two unknowns should be available.

The first equation can be derived from the first derivative of Eq. (3.15) at t_{k-1} as follows:

$$\frac{di''_{f_a}(t_{k-1})}{dt} = G_{II}\omega\cos(\omega t_{k-1} - \gamma_{II}) + (-\alpha'' e^{-\alpha'' t_{k-1}})(A_{1k}\cos\beta'' t_{k-1} + A_{2k}\sin\beta'' t_{k-1}) + (\beta'' e^{-\alpha'' t_{k-1}})(-A_{1k}\sin\beta'' t_{k-1} + A_{2k}\cos\beta'' t_{k-1}) \quad (A.1)$$

The previous equation can be rewritten as:

$$\frac{di''_{f_a}(t_{k-1})}{dt} = G_{II}\omega\cos(\omega t_{k-1} - \gamma_{II}) - A_{1k}\left(\alpha'' e^{-\alpha'' t_{k-1}}\cos\beta'' t_{k-1} + \beta'' e^{-\alpha'' t_{k-1}}\sin\beta'' t_{k-1}\right) + A_{2k}\left(-\alpha'' e^{-\alpha'' t_{k-1}}\sin\beta'' t_{k-1} + \beta'' e^{-\alpha'' t_{k-1}}\cos\beta'' t_{k-1}\right) \quad (A.2)$$

Applying Kirchoff's voltage law on the circuit of Case II as follows can drive the second equation needed to solve for A_{1k} & A_{2k}:

$$V_m \sin(\omega t) = R_f i''_{f_a}(t) + L_f \frac{i''_{f_a}(t)}{dt} + \frac{1}{C_f}\int i''_{f_a}(t)dt \quad (A.3)$$

Knowing that at:

$t = t_{k-1}$

$i''_{f_a}(t_{k-1}) = I_0$

$\frac{1}{C_f}\int i''_{f_a}(t_{k-1})dt = V_{c0}$

hence

$$V_m \sin(\omega t_{k-1}) = R_f I_0 + L_f \frac{i''_{f_a}(t_{k-1})}{dt} - L_f I_0 + V_{c0} \quad (A.4)$$

Then $\frac{di''_{f_a}(t_{k-1})}{dt}$ can be derived from the last equation as

$$\frac{di''_{f_a}(t_{k-1})}{dt} = \frac{1}{L_T}\left[V_m \sin(\omega t_{k-1}) - R_T I_0 + L_T I_0 - V_{on}\right] \tag{A.5}$$

By substituting from Eq. (A.5) into Eq. (A.2) we can get the one equation in the two unknowns A1k & A2k as follows:

$$C_1 = C_2 - C_3 A_{1k} + C_4 A_{2k} \tag{A.6}$$

where

$$C_1 = \frac{di''_{f_a}(t_{k-1})}{dt}$$

$$C_2 = G_{II}\omega\cos(\omega t_{k-1} - \gamma_{II})$$

$$C_3 = \alpha'' e^{-\alpha'' t_{k-1}}\cos|\beta|t_{k-1} + |\beta| e^{-\alpha'' t_{k-1}}\sin|\beta|t_{k-1}$$

$$C_4 = -\alpha'' e^{-\alpha'' t_{k-1}}\sin|\beta|t_{k-1} + |\beta| e^{-\alpha'' t_{k-1}}\cos|\beta|t_{k-1}$$

The second equation that relates the two unknowns A_{1k} & A_{2k} can be derived by calculating the current $i''_{f_a}(t)$ in Eq. (A.1) at t_{k-1} as follows:

$$i''_{f_a}(t_{k-1}) = G_{II}\sin(\omega t_{k-1} - \gamma_{II}) + e^{-\alpha'' t_{k-1}}\left(A_{1k}\cos|\beta|t_{k-1} + A_{2k}\sin|\beta|t_{k-1}\right) \tag{A.7}$$

which can be rewritten as

$$C_5 = C_6 + C_7 A_{1k} + C_8 A_{2k} \tag{A.8}$$

where

$$C_5 = i''_{f_a}(t_{k-1}) = I_0$$

$$C_6 = G_{II}\sin(\omega t_{k-1} - \gamma_{II})$$

$$C_7 = e^{-\alpha'' t_{k-1}}\cos\left(|\beta|t_{k-1}\right)$$

$$C_8 = e^{-\alpha'' t_{k-1}}\sin\left(|\beta|t_{k-1}\right)$$

Finally and by solving Eq. (A.6) and Eq. (A.9), A_{10} & A_{20} will have the final form as

$$A_{10} = \frac{\left(C_{10} - C_{20} \left(\frac{C_{10} - C_{20} - \frac{C_{12}}{C_{22}} (C_{20} - C_{21})}{\left(\frac{C_{12} C_{22}}{C_{22}} + C_{20} \right)} \right) \right)}{C_{11}} \qquad (A.11)$$

$$A_{20} = \frac{\left(C_{10} - C_{20} - \frac{C_{12}}{C_{22}} (C_{20} - C_{21}) \right)}{\left(\frac{C_{12} C_{22}}{C_{22}} + C_{20} \right)} \qquad (A.12)$$

Appendix B

Matlab Codes for the design procedure

This program is to investigate the change of the performance of the proposed SC scheme with the modified hysteresis control for both reactive power compensation and harmonic mitigation

```
Clear

% System frequency
f=60;
w=2*pi*f;

% Supply peak voltage
Vm=170;

% Time matrix
t=[0:0.00001e-0.2];
g=length(t);

% Reference current generation
Imdpr=10;
theta=pi/2;

Iref=Imd*_reactive(t,w,Imdpr,theta);  % reference reactive current

S1(1)=0;
S2(1)=0;

for n=1:g

%Filter resistance
RF=0.1;

%Filter inductance
LF=0.0022;
XLF=w*LF;
a*XLF=w*LF;

%Filter capacitance
CF=0.0005;
XCF=1/(w*CF);
```

```
%% constants
a1=0.07;
f1=60*0.9;
alpha2R=alpha(1);
R1=1/a/alpha2R;
alpha1=angle(1);

a2=0.07;
f2=60*0.9;
alpha2C=alpha(2);
R2=1/a/alpha2C;
alpha2=angle(2);

w0=1/sqrt(L*C);
B=sqrt(w0^2-a^2);
B=abs(B);


%% load resistance
R=100;

%Source impedance
Ls=0.001;
Rs=0.01;
Xs=w*Ls;
Zs=Rs+Xs*i;

Vrms=230;
srv=0.15;
sr=0.2;
reg=0.02;
Vdc=230;


%Initializing step
if n==1
   Icomp(k(1)=0.0;
   Vc1(k(1)=0.0;
   Vc2(k(1)=0.0;
   T0=t(1);
   Vcomp1=0.0;
   Vcomp2=0.0;
   error(n)=-Iref(1)+Icomp(k(1);
   Icompmag=0.0;
   Idiff(1)=Icompmag-Icomp(k(1);
```

```
Ifcurrmag1=Ifc1*sin(w*T1-alpha1);

diff=(Vm*sin(w*(t+t1)-fi)*Icomplx(x)-Ic1*Icomplx(x)-Vc1(k-1))/L1;
        C1(i)=diff;
        C2(i)=R2*w*cos(w*(t+t1-alpha2));
        C3(i)=a2*exp(-a2*(t+t1))*cos(B*(t+t1))+exp(-a2*(t+t1))*B*sin(B*(t+t1));
        C4(i)=-a2*exp(-a2*(t+t1))*sin(B*(t+t1))+exp(-a2*(t+t1))*B*cos(B*(t+t1));
        C5(i)=Icomplx(i);
        C6(i)=R2*sin(w*(t+t1-alpha2));
        C7(i)=exp(-a2*(t+t1))*cos(B*(t+t1));
        C8(i)=exp(-a2*(t+t1))*sin(B*(t+t1));
        A2(i)=(C5(i)*C6(i)-C7(i)*C5(i)*C2(i)-C1(i)))/(C7(i)*C4(i)*C3(i)-C8(i));
        A1(i)=(C2(i)-C1(i)-C4(i)*A2(i))/C3(i);


else

  diff(i)=diff1(i-1);
  Icomplx(i)=Icomplx(i-1);
  Vc1(i)=Vc1(i-1);
  Vc2(i)=Vc2(i-1);
  err=x(i)-Ifc1(i)*Icomplx(i);
  Ifcurrmag1=Ifc1*sin(w*T1-alpha1);

    end

    x(i)=Vm*sin(w*(t+t1));

    x1(i)=(Vm*sin(w*(t+t1)))*0.2;


%Start of the logic

% Begining of the positive half cycle

if x(i) >= 0
        diff=(Vm*sin(w*T1)-fi)*Icomplx(i)-L1*Icomplx(i-1)-Vc1(i-1))/L1;
        C1(i)=diff;
        C2(i)=R2*w*cos(w*T1-alpha2);
        C3(i)=a2*exp(-a2*T1)*cos(B*T1)+exp(-a2*T1)*B*sin(B*T1);
        C4(i)=-a2*exp(-a2*T1)*sin(B*T1)+exp(-a2*T1)*B*cos(B*T1);
        C5(i)=Icomplx(i);
        C6(i)=R2*sin(w*T1-alpha2);
        C7(i)=exp(-a2*T1)*cos(B*T1);
        C8(i)=exp(-a2*T1)*sin(B*T1);
```

[illegible]

%Regulation

[illegible]

[illegible]

% Beginning of the first mode when [illegible]

[illegible]

[illegible]

[

```
S20=S2(n);


 T1=t(n);

Vc2(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A20,B))/
Cf+Vc20(n);
 Vcmagt2=Vc2(n);


elseif error(n)> -er &  error(n) < er

 if Idiff(n) < 0

  Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
            a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));
  Icomp3(n)=Icomp(n) ;

    T1=t(n);

 Vc1(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A20,B))/
 Cf+Vc10(n);
  Vcmagt1=Vc1(n);


 else

  dI0=(Vm*sin(w*T0)-Rf*Icomp0(n)+Lf*Icomp0(n)-Vc20(n))/Lf;
  C10=dI0;
  C20=K2*w*cos(w*T0-alpha2);
  C30=a2*exp(-a2*T0)*cos(B*T0)+exp(-a2*T0)*B*sin(B*T0);
  C40=-a2*exp(-a2*T0)*sin(B*T0)+exp(-a2*T0)*B*cos(B*T0);
  C50=Icomp0(n);
  C60=K2*sin(w*T0-alpha2);
  C70=exp(-a2*T0)*cos(B*T0);
  C80=exp(-a2*T0)*sin(B*T0);
  A20=(C50-C60-(C70/C30*(C20-C10)))/(C70*C40/C30+C80);
  A10=(C20-C10+C40*A20)/C30;

  Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
            a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));

  Icomp4(n)=Icomp(n);
```

```
            S2(n)=S20+1;
            S20=S2(n);


            T1=t(n);

          Vc2(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A20,B))/
          Cf+Vc20(n);
            Vcmagt2=Vc2(n);


          end
        end

% end of the first mode when 0<vs(t)<erv*Vm

% Beginning of the second mode when vs(t)>erv*Vm

elseif vs(n)>=erv*Vm
          if error(n) >= er
          Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
                  a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));
          Icomp5(n)=Icomp(n);

              S2(n)=S20+1;
              S20=S2(n);


            T1=t(n);

          Vc1(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A20,B))/
          Cf+Vc10(n);
          Vcmagt1=Vc1(n);


          elseif error(n) <= -er

            Icomp(n)=K1*sin(w*t(n)-alpha1)+(Icomp0(n)-
            Iforcmag1)*exp(a1*T0)*exp(-a1*t(n));
            Icomp6(n)=Icomp(n);
            S1(n)=S10+1;
            S10=S1(n);


          elseif error(n)> -er & error(n) < er
```

```
                    if  Idiff(n) < 0

                    Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
                              a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));
                    Icomp7(n)=Icomp(n) ;

                       T1=t(n);

                     Vc1(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A
                     20,B))/Cf+Vc10(n);
                        Vcmagt1=Vc1(n);


                    else

                    Icomp(n)=K1*sin(w*t(n)-alpha1)+(Icomp0(n)-
                              Iforcmag1)*exp(a1*T0)*exp(-a1*t(n));
                    Icomp8(n)=Icomp(n) ;


                    end
                end

      % End of the second mode when vs(t)>erv*Vm
     end


% End of the positive half cycle

% Begining of the negative half cycle


elseif vs(n) < 0
        dI0=(Vm*sin(w*T0)-Rf*Icomp0(n)+Lf*Icomp0(n)-Vc20(n))/Lf;
        C10=dI0;
        C20=K2*w*cos(w*T0-alpha2);
        C30=a2*exp(-a2*T0)*cos(B*T0)+exp(-a2*T0)*B*sin(B*T0);
        C40=-a2*exp(-a2*T0)*sin(B*T0)+exp(-a2*T0)*B*cos(B*T0);
        C50=Icomp0(n);
        C60=K2*sin(w*T0-alpha2);
        C70=exp(-a2*T0)*cos(B*T0);
        C80=exp(-a2*T0)*sin(B*T0);
        A20=(C50-C60-(C70/C30*(C20-C10)))/(C70*C40/C30+C80);
        A10=(C20-C10+C40*A20)/C30;
```

```
%Regulation
 if ((vs(n)<0)&(vs(n)>-reg*Vm))
        Vc20(n)=-Vdc;
      end

% Begining of the third mode when -erv*Vm<vs(t)<0.0

      if ((vs(n)<0)&(vs(n)>-erv*Vm))
            if    error(n)<=-er
                  Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
                        a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));
                  Icomp9(n)=Icomp(n);
                  S2(n)=S20+1;
                        S20=S2(n);

                           T1=t(n);

                   Vc2(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A
                   20,B))/Cf+Vc20(n);
                    Vcmagt2=Vc2(n);


            elseif  error(n)>=er

                  dI0=(Vm*sin(w*T0)-Rf*Icomp0(n)+Lf*Icomp0(n)-Vc10(n))/Lf;
                  C10=dI0;
                  C20=K2*w*cos(w*T0-alpha2);
                  C30=a2*exp(-a2*T0)*cos(B*T0)+exp(-a2*T0)*B*sin(B*T0);
                  C40=-a2*exp(-a2*T0)*sin(B*T0)+exp(-a2*T0)*B*cos(B*T0);
                  C50=Icomp0(n);
                  C60=K2*sin(w*T0-alpha2);
                  C70=exp(-a2*T0)*cos(B*T0);
                  C80=exp(-a2*T0)*sin(B*T0);
                  A20=(C50-C60-(C70/C30*(C20-C10)))/(C70*C40/C30+C80);
                  A10=(C20-C10+C40*A20)/C30;

                      Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
                            a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));
                      Icomp10(n)=Icomp(n);
                      S2(n)=S20+1;
                         S20=S2(n);


                      T1=t(n);
```

```
Vc1(n)=+(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A20,B))
/Cf+Vc10(n);
Vcmagt1=Vc1(n);


elseif error(n)> -er &  error(n) < er

        if Idiff(n) > 0

            Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
                    a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));
            Icomp11(n)=Icomp(n) ;

             T1=t(n);

           Vc2(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A
           20,B))/Cf+Vc20(n);
            Vcmagt2=Vc2(n);


        else

       dI0=(Vm*sin(w*T0)-Rf*Icomp0(n)+Lf*Icomp0(n)-Vc10(n))/Lf;
       C10=dI0;
       C20=K2*w*cos(w*T0-alpha2);
       C30=a2*exp(-a2*T0)*cos(B*T0)+exp(-a2*T0)*B*sin(B*T0);
       C40=-a2*exp(-a2*T0)*sin(B*T0)+exp(-a2*T0)*B*cos(B*T0);
       C50=Icomp0(n);
       C60=K2*sin(w*T0-alpha2);
       C70=exp(-a2*T0)*cos(B*T0);
       C80=exp(-a2*T0)*sin(B*T0);
       A20=(C50-C60-(C70/C30*(C20-C10)))/(C70*C40/C30+C80);
       A10=(C20-C10+C40*A20)/C30;

            Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
                    a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));
            Icomp12(n)=Icomp(n);
            S2(n)=S20+1;
               S20=S2(n);


            T1=t(n);
```

```
                Vc1(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A
                20,B))/Cf+Vc10(n);
                 Vcmagt1=Vc1(n);


                end

        end

% end of the third mode

% Beginning of the fourth mode when vs(t)<-erv*Vm

elseif vs(n)<=-erv*Vm
            if  error(n) <= -er
                Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
                        a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));
                Icomp13(n)=Icomp(n);

                S2(n)=S20+1;
                S20=S2(n);



                T1=t(n);

                 Vc2(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A
                 20,B))/Cf+Vc20(n);
                 Vcmagt2=Vc2(n);



              elseif  error(n) >= er

                Icomp(n)=K1*sin(w*t(n)-alpha1)+(Icomp0(n)-
                        Iforcmag1)*exp(a1*T0)*exp(-a1*t(n));
                Icomp14(n)=Icomp(n);
                T1=t(n);
                S1(n)=S10+1;
                S10=S1(n);



              elseif  error(n)>-er &  error(n) < er
```

```
if Idiff(n) > 0

    Icomp(n)=K2*sin(w*t(n)-alpha2)+exp(-
            a2*t(n))*(A10*cos(B*t(n))+A20*sin(B*t(n)));
    Icomp15(n)=Icomp(n) ;

    T1=t(n);

  Vc2(n)=(quad8('CapI1',T0,T1,[],[],K2,w,alpha2,a2,A10,A
  20,B))/Cf+Vc20(n);
   Vcmagt2=Vc2(n);


else

    Icomp(n)=K1*sin(w*t(n)-alpha1)+(Icomp0(n)-
            Iforcmag1).*exp(a1*T0)*exp(-a1*t(n));
    Icomp16(n)=Icomp(n) ;


 end

end

 % End of the second mode when vs(t)<-erv*Vm
end



% End of the negative cycle

end
% End of logic


Icompmagt=Icomp(n);
Idiffmagt=Icompmagt-Icomp0(n);
T0=t(n);
Icompv(n)=Icomp(n)*4;

if vs(n) >= 0
  Vc20(n)=Vcmagt2;
  Vc201(n)=Vcmagt2*0.2;
```

```
else
  Vc10(n)=Vcmagt1;
  Vc101(n)=Vcmagt1*0.2;

  end


end
```

```
start = round(length(t)/2);  % Choice is made based on steady state
   % operation

TSUPPLY=1/f;

i = 1;
while (abs(t(start + i) - t(start)) <= TSUPPLY)
    fs1(i) = S1(start + i);
    fs2(i) = S2(start + i);
    i = i + 1;
end
    fs1max=max(fs1);

    j1=length(fs1);

for i1=1:j1
   if fs1(i1)>0
   Fs1=(fs1max-fs1(i1))*60
   break
   end
end



waveforms = Icomp;
i = 1;

while (abs(t(start + i) - t(start)) <= TSUPPLY)
    waves(i) = waveforms(start + i);
    i = i + 1;
end

    LEN = i-1;      % Number of sample points corresponding to a
                % single cycle
    freq = 1:LEN/2;
    freq = freq -1; % Frequency points on X-axis
    wave_single_cycle = waves(1:LEN);      % time domain signal
```

```
I_FFTm = 2/(LEN)*abs(fft(wave_single_cycle));
   % Computation of FFT

I_FFTa = angle(fft(wave_single_cycle)); % Computation of angle


for i = 1:LEN/2,

    I_FFT(i)= I_FFTm(i);    % The first half of the samples
  % carry the necessary frequency information

  % The second half is redundant and discarded

    I_percent(i)= I_FFTm(i)/I_FFTm(2)*100;
   %percentage of fundamental

    I_ang(i)= I_FFTa(i)*180/pi; %Compuation of the angle


    IHD(i)=I_FFTm(i)/I_FFTm(2)*100;
end

FFTs(1:length(I_FFT)) = I_FFT;

% Plotting the results
%bar(freq,FFTs(1:LEN/2));
%grid;
%axis([0 17 0 170]);

%xlabel('Harmonic Number - n'); ylabel('FFT');

% Computation of total harmonic distortions
% Only the odd harmonics are used for FFT computation
% zeros(1,5)
 THD = 0;

 Irms1=0;


 for i = 1:1:19,

    Irms1= Irms1+ I_FFT(i)*I_FFT(i)/2;

 end
```

```
Irms=sqrt(Irms1);


THDr = abs(sqrt(Irms^2-((I_FFT(2)/sqrt(2))^2))/Irms*100)
THDf=abs(sqrt(Irms^2-
        ((I_FFT(2)/sqrt(2))^2))/I_FFT(2)*sqrt(2)*100)



% End of the  "For loop"
zoom on

%figure(1)
%subplot(2,1,1)
%plot(t,Vc10,t,vs,t,Vc20);grid
%subplot(2,1,2)
%plot(t,Icomp);grid

%figure(2)
%plot(t,Vc10,t,vs,t,Vc20,t,Icompv);grid
```